PROGRAM
September 14 – 18, 2015
Graz, Austria
45th European Solid-State Device Research Conference

Messe Congress
Graz, Austria
September 14 – 18, 2015

Organized by:
JOANNEUM RESEARCH
Forschungsgesellschaft mbH
Graz, Austria

Technical Co-Sponsorship:

IEEE
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With headquarters in Austria, ams employs over 1,800 people globally and serves more than 8,000 customers worldwide. Analog sensor development is done in 14 design centers around the globe and ams operates an in-house 8 inch wafer fab in Austria and a test facility at the Philippines. ams is listed on the SIX Swiss stock exchange (ticker symbol: AMS). More information about ams can be found at www.ams.com.

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Infineon Technologies AG is a world leader in semiconductor solutions. We make life easier, safer and greener – with technology that achieves more, consumes less and is accessible to everyone.

Our innovative solutions optimize the generation, transmission and consumption of power, for instance, also maximizing energy efficiency in everything from lighting to industrial drives. In addition, we are enabling the development of cars and vehicles offering greater energy efficiency, functionality and safety. And our robust security solutions create an anchor of trust in today’s computing devices, protecting the integrity, authenticity and confidentiality of information as it travels across the Internet of Things.

Microelectronics from Infineon is the key to a better future.

Contact
DI Stefan Rohringer, Vice President
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NXP Semiconductors N.V. (NASDAQ: NXPI) creates solutions that enable secure connections for a smarter world. Building on its expertise in high-performance mixed signal electronics, NXP is driving innovation in the areas of connected car, security, portable & wearable, and the Internet of Things.

We focus on developing innovative products, systems and sub-system that allow our customers to bring their end products to market more quickly. Our products, particularly our application system and sub-system solutions, help our customers design critical parts of their end products and thus help many of them to differentiate themselves based on feature performance, advanced functionality, cost or time-to-market. We leverage our technical expertise in the areas of RF, analog, power management, interface, security technologies and digital processing across our priority applications markets.

Our Standard Products business supplies a broad range of standard semiconductor components, such as small signal discretes, power discretes, protection and signal conditioning devices and standard logic devices.

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Web: www.nxp.com
Science, passion, technology

Graz University of Technology has built up an impressive record of achievements in teaching and research over 200 years. Five Fields of Expertise, internationalisation, and co-operations with science and industry go to form the profile of TU Graz.

Currently, some 12,800 students from almost 80 countries take advantage of a full range of science and engineering subjects in seven faculties and more than 100 institutes. Around 2,400 graduates leave the University each year and find superb career opportunities on the job market. The powerful network of Graz University of Technology with industry, business and research leads to extraordinarily successful co-operations. The future-oriented focus of TU Graz is its carefully implemented internationalisation. With the conversion of PhD and master’s programmes into English, students are ideally equipped for the global market place. Added to this are strategic co-operations with internationally chosen leading universities.

Contact
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Email: info@tugraz.at
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Chair’s Message
On behalf of the Organizing Committee of ESSDERC 2015, it is our pleasure to welcome you to the 45th European Solid-State Device Research Conference. ESSDERC 2015 runs in parallel to its sister conference ESSCIRC 2015, covering all aspects of modern solid-state systems, circuits and devices at a single event. The increasing level of integration for system-on-chip design made available by advances in integration technology is stimulating more than ever before the need for deeper interaction among technologists, device experts, circuit designers and system architects. As a participant at ESSDERC and ESSCIRC, you will have the opportunity to learn of the latest advances in these fields, and to meet those who have dared, pioneered and succeeded.

The conference takes place in the “Messe Congress Graz” conference center near the center of Graz, the workshop day will be hosted at the nearby campus of the Graz University of Technology. The city of Graz has a long tradition as a university city and offers cultural highlights, ranging from architecture, music and theatre to design and the fine arts.

This year, a total of 107 submissions originating from 23 countries were received for ESSDERC coming from the following areas: 70 papers from Europe, 28 from Asia-Pacific, 7 from North-America and 1 from Middle East. This is proof of the truly international nature of ESSDERC. The Technical Program Committee with 105 world-class experts from academia and industry selected 59 papers for oral presentations. In course of the opening on Tuesday morning a panel discussion with highly experienced leaders on the topic “European Microelectronics - Leading in Automotive?” will be held and give insight into this important segment of the semiconductor market. Nine plenary and joint plenary presentations by outstanding guest speakers enhance the program, focusing on highly relevant topics. Following the last year’s idea, 6 focus sessions on specific topics have been added. We are also hap-
Welcome to ESSDERC 2015

It is my pleasure to announce this year’s closing session “Synchronous Advancement of Hardware and Software – Added Value for Europe?” which will be jointly organized by ESSCIRC/ESSDERC and the stakeholders of ECSEL.

In addition to three days of oral presentations, a day dedicated to introductory tutorials precedes the technical sessions, while a day devoted to workshops follows, presenting work currently carried out by European research consortia.

We are extremely proud to have the collaboration of an exceptional team of the Organizing Committee and of the Technical Program Committee, who have all worked very hard. We are hugely indebted to all these volunteers. Our warm thanks to all of them for their dedication, enthusiasm and professionalism.

We would also like to thank the Steering Committee of ESSDERC/ESSCIRC for giving us the opportunity to organize this event and for many valuable recommendations and discussions.

Last but not least, we would like to express our greatest appreciation to all the authors who submitted papers to the conference and to all delegates, tutorial lecturers and plenary speakers who have travelled to Graz to interact and share their thoughts during the conference.

Enjoy the 2015 edition of ESSDERC/ESSCIRC and your visit to Graz, and we hope to see you all back next year in Lausanne, Switzerland, for ESSDERC/ESSCIRC 2016!

Welcome!

Wolfgang Pribyl
Conference Chair – ESSDERC/ESSCIRC 2015

Martin Schrems, Tibor Grasser
TPC chairs – ESSDERC 2015
<table>
<thead>
<tr>
<th>CONTENTS</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>ESSDERC Schedule</td>
<td>11</td>
</tr>
<tr>
<td>Meeting Rooms</td>
<td>15</td>
</tr>
<tr>
<td>Program at a Glance</td>
<td>19</td>
</tr>
<tr>
<td>Committees</td>
<td>24</td>
</tr>
<tr>
<td>Conference Venue</td>
<td>30</td>
</tr>
<tr>
<td>Social Program</td>
<td>35</td>
</tr>
<tr>
<td>General Information</td>
<td>38</td>
</tr>
<tr>
<td>Conference Overview</td>
<td>41</td>
</tr>
<tr>
<td>Joint Plenary Talks</td>
<td>44</td>
</tr>
<tr>
<td>ESSDERC Plenary Talks</td>
<td>54</td>
</tr>
<tr>
<td>ESSDERC Tutorials</td>
<td>58</td>
</tr>
<tr>
<td>Workshops</td>
<td>62</td>
</tr>
<tr>
<td>ESSDERC Technical Program</td>
<td>77</td>
</tr>
<tr>
<td>Author Index</td>
<td>105</td>
</tr>
</tbody>
</table>
Monday, September 14, 2015

Tutorials

10:50 – 18:15
ESSDERC Tutorial:
**GaN Based Power Electronics**
Organizer: Oliver Häberlen, Infineon Technologies, Austria

13:00 – 18:45
ESSDERC Tutorial:
**Novel Transistors – Beyond the Planar Silicon MOSFET**
Organizer: Max Lemme, University of Siegen, Germany

Tuesday, September 15, 2015

08:40 – 09:00  Conference Opening
09:00 – 10:20  Joint Plenary Lectures
10:20 – 10:40  *Coffee Break*
10:40 – 11:20  Joint Plenary Lecture
11:20 – 12:20  Panel
12:20 – 13:20  *Lunch*
13:20 – 14:00  ESSCIRC Plenary Lecture
14:00 – 15:40  Technical Sessions
                 Focus Session
15:40 – 16:00  *Coffee Break*
16:00 – 18:00  Technical Sessions
18:00 – 19:00  Young Professionals Networking Event
19:00  *Welcome Reception*
Wednesday, September 16, 2015

08:40 – 10:00 Joint Plenary Lectures
10:00 – 10:20 Awards
10:20 – 10:50 Coffee Break
10:50 – 12:10 Technical Session
12:10 – 13:20 Lunch
13:20 – 15:20 Technical Session
15:20 – 15:40 Coffee Break
15:40 – 16:20 ESSDERC Plenary Lecture
16:20 – 18:00 Technical Sessions
18:00 – 19:00 2016 TPC Meeting (by invitation only)
19:40 Gala Dinner

Thursday, September 17, 2015

08:40 – 10:00 Joint Plenary Lectures
10:00 – 10:20 Preview on ESSCIRC/ESSDERC 2016
10:20 – 10:50 Coffee Break
10:50 – 12:10 Technical Sessions
12:10 – 13:20 Lunch
13:20 – 14:00 ESSDERC Plenary Lecture
14:00 – 15:40 Technical Sessions
15:40 – 16:00 Coffee Break
16:00 – 16:20 Joint Plenary Lecture
16:20 – 17:40 Closing Session
19:00 Guided City Tour through Graz
Friday, September 18, 2015

Workshops
(Venue: Graz University of Technology, Campus Inffeldgasse)

08:30 – 16:00
MOS-AK: Enabling Compact Modeling R&D Exchange
Chair: Wladek Grabinski, MOS-AK (EU)

08:45 – 16:00
SINANO Workshop: New Materials for Nanoelectronics
Chair: Enrico Sangiorgi, University of Bologna

08:45 – 12:30
RFID Technologies Exploiting 2D and 3D Printing and Packaging Techniques
Chair: Jasmin Grosinger, Graz University of Technology

14:00 – 17:30
From Atom to Transistor – Models and Techniques for Predictive Simulation of Emerging Devices
Chair: Zlatan Stanojević, Global TCAD Solutions GmbH

08:45 – 12:30
Variation-Aware Design for RF Engineers
Chair: Stephan Weber, Cadence Design Systems

14:00 – 17:30
Electromagnetic Compatibility of Integrated Circuits
Chair: Bernd Deutschmann / Gunter Winkler, Graz University of Technology
08:45 – 15:30
Variability – From Equipment to Circuit Level
Chair: Jürgen Lorenz, Fraunhofer IISB

08:30 – 13:00
DC-DC Converter Techniques
Chair: Christoph Sandner, Infineon
Inffeldgasse 25 D / ground floor
Meeting Rooms, University of Technology

Inffeldgasse 25 D / first floor
Inffeldgasse 12 / ground floor

WORKSHOP ROOM

6
<table>
<thead>
<tr>
<th>Room &quot;Main&quot;</th>
<th>Start</th>
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<th>Room &quot;Foyer&quot;</th>
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<th>Room &quot;Salon&quot;</th>
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<th>Room &quot;Bar&quot;</th>
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<tr>
<td>11:00-12:30</td>
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<td>Intro by the Chair Officer</td>
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<td>14:00-16:00</td>
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<td>RF Design in BiCMOS: Physical Design of Bipolar Transistors for MM-Wave Circuits</td>
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<td>Novel Transistors – Beyond the Planar Silicon MOSFET: Growth of III-V on Silicon Wafer</td>
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<td>Novel Transistors – Beyond the Planar Silicon MOSFET: 3D Integrated Devices</td>
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<td>15:30-17:30</td>
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<td>Novel Transistors – Beyond the Planar Silicon MOSFET: Graphene Field-Effect Transistors for Circuit Design</td>
<td>18:30</td>
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**Program at a Glance**

Monday, September 14, 2015 – Tutorials

11:00-12:30: Introduction to the Real World
12:30-13:10: Coffee Break
13:10-13:30: Lunch
13:30-14:00: Coffee Break
14:00-14:30: Coffee Break
14:30-15:00: Coffee Break
15:00-15:30: Coffee Break
15:30-16:00: Coffee Break
16:00-16:30: Coffee Break
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<tr>
<th>Time</th>
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<tr>
<td>08:40-09:00</td>
<td>Coffee Break</td>
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<tr>
<td>09:00-10:20</td>
<td>Joint Plenary Lectures (Room Graz): J. Dickmann, Dairiger AG, P. Leitnerer, Infineon Technologies</td>
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<tr>
<td>11:20-12:20</td>
<td>Lunch</td>
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<tr>
<td>12:20-13:20</td>
<td>Focus Session: TECHNOLOGY, DESIGN AND CHARACTERIZATION OF WIDE BANDED POWER DEVICES (Part 1)</td>
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<td>13:20-14:00</td>
<td>Compact Models</td>
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<td>14:00-15:40</td>
<td>Focus Session: FILTERS AND OPTICAL LINKS</td>
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<td>15:40-16:00</td>
<td>Coffee Break</td>
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<tr>
<td>16:00-17:40</td>
<td>Digital Circuits and Systems</td>
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<td>17:40-18:00</td>
<td>Welcome reception</td>
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<td>18:00-19:00</td>
<td>Young Professionals Mentoring and Career Coaching Event (Room Graz)</td>
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<td>19:00-21:00</td>
<td>Welcome reception</td>
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<tr>
<td>08:40</td>
<td>Joint Plenary Lectures (Room Graz):</td>
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<td>B. Stadlober, JOANNEUM RESEARCH</td>
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<td>09:00</td>
<td>Preview ESSCIRC/ESSDERC 2016 (Room Graz)</td>
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<td>10:20</td>
<td>Coffee Break</td>
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<td>10:50</td>
<td>Modeling of Important Issues for Main Stream Silicon Devices</td>
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<td>Advanced CMOS Device and Technology</td>
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<td>Resistive RAM</td>
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<td>10:50</td>
<td>Invited Session: Sensors and MEMS Applications</td>
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<td>ESSCIRC Plenary (R. Graz): Y. Deval, Univ. of Bordeaux</td>
</tr>
<tr>
<td>14:00</td>
<td>Invited Session (R. Klagenfurt): Advanced Biomedical Devices</td>
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<td>Characterization of Advanced Devices</td>
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<td>Advanced Numerical Modeling of Alternative Material Devices</td>
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<td>15:40</td>
<td>Coffee Break</td>
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<td>16:00</td>
<td>Joint Plenary Lecture (Room Graz): W. van Pyambreoeck, DG CONNECT</td>
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<td>16:20</td>
<td>Closing Session: Synchronous Advancement of Hardware and Software – Added Value for Europe? (Room Graz)</td>
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<td>19:00</td>
<td>Guided City Tour through Graz</td>
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</tbody>
</table>

**Program at a Glance**

**Friday, September 18, 2015**
COMMITTEES

Organizing Committee

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JOANNEUM RESEARCH

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Infineon Technologies Austria AG

Thomas Stockmeier
ams AG

Volker Graeger
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Tibor Grasser
Vienna University of Technology

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IBM Research Zurich

Workshop Chair  Mario Auer
Graz University of Technology

Tutorials Chairs  Gernot Hueber
NXP Semiconductors Austria

Tibor Grasser
Vienna University of Technology
<table>
<thead>
<tr>
<th>Role</th>
<th>Names and Affiliations</th>
</tr>
</thead>
<tbody>
<tr>
<td>Committees</td>
<td></td>
</tr>
<tr>
<td>Communication/ Publicity Chair</td>
<td>Alexandra Reischl, JOANNEUM RESEARCH</td>
</tr>
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<td>Gernot Hueber, NXP Semiconductors Austria</td>
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<tr>
<td>Sponsoring Chair</td>
<td>Wolfgang Pribyl, JOANNEUM RESEARCH</td>
</tr>
<tr>
<td>Financial Chairs</td>
<td>Renate Reinisch, JOANNEUM RESEARCH</td>
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<td>Gabriele Katz, JOANNEUM RESEARCH</td>
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<td>Incoming Chairs</td>
<td>Christian Enz, École polytechnique fédérale de Lausanne (EPFL)</td>
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<td>Heike Riel, IBM Research Zurich</td>
</tr>
<tr>
<td>Logistic / Exhibition Chair</td>
<td>Birgit Kößler, JOANNEUM RESEARCH</td>
</tr>
<tr>
<td>Local Scientific Secretariat</td>
<td>JOANNEUM RESEARCH</td>
</tr>
<tr>
<td>Local Registration Secretariat</td>
<td>SISTEMA Congressi s.r.l.</td>
</tr>
<tr>
<td>Website and Paper Selection Site</td>
<td>JOANNEUM RESEARCH</td>
</tr>
</tbody>
</table>
COMMITTEES

Steering Committee

Ralf Brederlow  Texas Instruments, Germany (Chair)
Andreia Cathelin  STMicroelectronics, France (Vice-Chair)
Cor Claeys  Imec, Belgium (Executive Secretary)

Piero Andreani  Lund University, Sweden
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Bram Nauta  University of Twente, The Netherlands
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Andrea Redaelli   Micron
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Dimitris Tsoukalas National Technical University of Athens
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David Wright      University of Exeter
### MEMS, Sensors & Display Technologies

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<tr>
<td>Mirjana Banjevic</td>
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<td>Wolfgang Benecke</td>
<td>Fraunhofer ISIT</td>
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<td>Cesare Buffa</td>
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<td>Joachim Burghartz</td>
<td>IMS CHIPS</td>
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<td>Volker Cimalla</td>
<td>Fraunhofer IAF, TU Imenau</td>
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<td>Piet De Moor</td>
<td>IMEC</td>
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<td>Piotr Grabiec</td>
<td>ITE Warsaw</td>
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<td>Yasar Gurbuz</td>
<td>Sabanci University</td>
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<td>Sebastien Hentz</td>
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<td>Jong Kim</td>
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<td>Christoph Kutter</td>
<td>Fraunhofer EMFT</td>
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<td>Raluca Muller</td>
<td>IMT Bucharest</td>
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<td>Radu Sporea</td>
<td>University of Surrey</td>
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### Emerging Non-CMOS Devices & Technologies

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<tr>
<td>Max Lemme</td>
<td>University of Siegen (Chair)</td>
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<td>Jong-Hyun Ahn</td>
<td>Yonsei University, Seoul</td>
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<td>Costin Anghel</td>
<td>ISEP</td>
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<td>Kees de Groot</td>
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<td>Elena Gnani</td>
<td>University of Bologna</td>
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<td>Steve Hall</td>
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<td>Ryoichi Ishihara</td>
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<td>Mikael Oestling</td>
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<td>Tomas Palacios</td>
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<td>Andreas Schenk</td>
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<td>Takagi Shinichi</td>
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<td>Thomas Skotnicki</td>
<td>STMicroelectronics</td>
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<td>Joseph Tringe</td>
<td>LLNL</td>
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<td>Thomas Zimmer</td>
<td>University of Bordeaux</td>
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Welcome to Graz

Graz has a population of approximately 270,000, making it the second-largest city in Austria. Geographically speaking, Graz is situated in a basin which opens to the hilly countryside of the Styrian wine-growing region in the south and which is bordered by the alpine pastures of the eastern foothills of the Alps in the north.

It is the capital of the federal province of Styria and a tourist hotspot for people from all over the world. Graz has a long tradition as a university city and its four universities and two universities of applied sciences are home to more than 44,000 students.

The historic city centre of Graz belongs to one of the best-preserved historic city centres in Central Europe. The “Kunsthaus” (art exhibition center) and the floating island in the Mur, which was opened in 2003 when Graz was the Cultural Capital of Europe, stand for a whole range of additional examples.

The city appears lively and constantly in motion with regard to all cultural aspects; not only in its architecture, but in music, theater, literature, design and the fine arts. Don’t miss the opportunity discover also the unique surroundings of this beautiful part of Austria!
Messe Congress Graz
The ESSCIRC/ESSDERC Conference and the Tutorials Day from 14 to 17 September 2015 will take place at the:

Messe Congress Graz Betriebsgesellschaft m.b.H.
Messeturm, Messeplatz 1, 8010 Graz, Austria
Phone: +43 316 8088-0, office@mcg.at, www.mcg.at

Messe Congress Graz is uncompromisingly contemporary with a total of 13,000 sqm of floor space. Visitors enter the building under a canopy that projects 47 m into the street making sure that even on rainy days their way to the meeting stays dry and comfortable. Facilities include a total of 25 seminar rooms and plenary halls ranging from 50 to 6,500 sqm, VIP café, terrace, press club and video conferencing room.

How to reach the venue:
- Only 10 km from Graz Airport
- Only 1.5 km from the Graz-Ost motorway exit
- Parking for 2,000 cars on the Messegelände site/underground car park
- Public transport: Tram stops on lines 4, 5, 6 Stations: Jakominigürtel/Messe, Stadthalle, Fröhlichgasse/Messe, Münzgrabenstraße/Messe
- Taxi rank in front of the venue
Graz University of Technology
The Workshop Day (Friday, 18 September, 2015) will take place at the:

Graz University of Technology
Campus Inffeldgasse

How to reach the venue:
• Only 10 km from Graz Airport
• Only 4 km from the Graz-Ost motorway exit
• Parking in the area Petersgasse/Sandgasse
• Public transport: Tram stops on line 6
  Station: St. Peter - Schulzentrum

Public Transport – GVB tickets:
24 h  EUR  4.80
7 days  EUR 13.40

Taxi Phone Numbers:
• +43 316 878
• +43 316 889
• +43 316 2801
Useful information for a stay in Austria

Banks - Currency
All banks in Austria exchange foreign currency and traveller's cheques. Banks are open from Monday to Tuesday from 08.30 to 12.30 and 13.30 to 16.00. On Friday they are open from 08.30 to 14.30. The local currency is € (Euro). There is no restriction on the import of foreign currency into Austria and there are no limits for traveller's cheques. Automatic teller machines and exchange offices are readily available. Most hotels, restaurants and shops accept major credit cards but check first!

Mail and telecommunication
Post offices display the sign "POST" on a yellow background. At a PT office you can telephone, send mail, telegrams and faxes. For local calls you can buy phone cards there or in any tobacconist. When calling abroad from Austria, you must first dial the International code "00", then country code and private number. Austrian Country Code is +43 and Graz City Code is (0)316.

Emergency numbers:
- Police 133
- Ambulance 144
- Fire 122

Electricity
Electricity in Austria is 230 volts. If you plan on using your own 110 volt appliances, you will need a voltage converter, unless your appliance is designed to also work with 230 volts electricity (dual voltage). Voltage converters might not be always easy to find, and definitely, you don't want to bother with looking for one while you should be working, sightseeing or relaxing. If
you think you will need one, it is a good idea to get it before you leave home. Regardless of voltage, if your appliance has flat prongs, you will need a plug adapter: Austrian sockets are designed to accept round prongs. Do get one before your leave!

Tipping
Tipping up to 10% for outstanding service is of course accepted, but not necessarily expected in Austrian restaurants, hotels and taxis.

Climate
Due to its geographic position, Graz enjoys a pleasant climate with mediterranean influences year-round. September could be very warm, but also cold and humid. Please check the current weather on www.wetter.at. Remember meeting room temperatures and personal comfort zones vary widely. It is recommended that you bring a sweater or jacket to the sessions.
Welcome Reception
Tuesday, 15 September, 2015 – 19:00

On Tuesday, 15 September, 2015 the Welcome Reception will greet the conference attendees in the "Nikola Tesla Hall" (Test Laboratory of High Voltage Engineering Graz) at the Institute of High Voltage Engineering and System Performance, Graz University of Technology. In honor of the 150th birthday of Nikola Tesla, who started his scientific career at the Graz University of Technology, the “Hochspannungshalle” (high voltage laboratory) has been renamed into "Nikola Tesla lab", which serves for experiments in high voltage and power distribution projects. From time to time it is used as location for special events. About 500 mainly successful inventions, e.g. the concept of alternating current, trace back to Nikola Tesla.

"Nikola Tesla Hall" -
Graz University of Technology
Inffeldgasse 18, 8010 Graz

For all registered attendees.
Complimentary shuttle service will be provided.
Gala Dinner
Wednesday, 16 September, 2015 – 19:40

Dinner Speech: “Security – Risks and Challenges” by Reinhard Posch, Graz University of Technology and Chief Information Officer of the Republic of Austria

On Wednesday, 16 September, 2015, the Gala Dinner will take place in the beautiful “Seifenfabrik” (Soap Factory). The “Seifenfabrik” is a former redbrick soap factory, built in 1872. Located not far away from the city centre this location today is protected under the preservation law for historic buildings and monuments. It is embedded into the green surroundings of the river Mur. The “Fachwerkhalle” (700 sqm) with its wooden structure of the ceiling and the red brick walls give this room a special atmosphere.

"Seifenfabrik"
Angergasse 41-43, 8010 Graz

For all registered attendees.
Complimentary shuttle service will be provided.
Guided City Walk by Night
Thursday, 17 September, 2015
Special event 19:00 to 21:00

Graz by night enchants. Walk through narrow lanes lit by antique lanterns, city facades glowing in the evening light. Encounter the mesmerizing flashing lights of an alien and a glowing island. See Graz in a different light.

Meeting Point:
Hauptplatz “main place”, in front of the City Hall
GENERAL INFORMATION

Registration time
Monday  09:00 – 19:00
Tuesday 08:00 – 19:00
Wednesday 08:00 – 19:30
Thursday 08:00 – 18:30
Friday  08:00 – 18:00

Language
The official language of the meeting is English: no simultaneous translation available.

Webpages
ESSCIRC 2015 webpage: www.esscire2015.org
ESSDERC 2015 webpage: www.essderc2015.org

Name Badges
Badges must always be visibly worn during the scientific session, coffee breaks and lunches at the conference site but also during social program and extra activities.

Internet Access / Wi-Fi
Free wireless internet access will be available on site.

Certificate of attendance
Certificates will be given on request to all registered participants at the registration desk at the end of the meeting.

Speakers Briefing
Authors should meet their chairperson in the session room 15 minutes ahead the respective sessions.

Conference Proceedings
All participants will receive an USB stick containing the accepted papers for both ESSCIRC and ESSDERC. Printed proceedings will be available on request (35 € each).
Best Paper Award
Papers at the conferences will be considered for the Best Paper Award and for the Best "Young Scientist" Paper Award. The selection will be based on the results of the paper selection process and the judgement of the chairmen. Award delivery will take place at ESSCIRC/ESSDERC 2016.

Coffee breaks and lunches
Coffee breaks and lunches will be served free of charges at the conference to fully registered participants wearing their badges.
Accompanying persons have no access to scientific session nor to coffee breaks and lunches.
Please note that vegetarian dishes will be on the daily menu; for other special needs, we will try to serve a good variety of food so that it will be easier for you to get some alternatives in case of special diet restriction.

Smoking policy
Participants are requested to refrain from smoking inside the Messe Congress Graz.

Insurance Disclaimer / Liability
In registering for the Conference, participants agree that neither the Scientific/Organizing Committees nor the Organizing Secretariat assumes any liability. Participants should therefore organize their own health and travel insurance.

Persons with special needs
Every effort has been made to ensure that people with special needs are catered for during the conference. Should you require any specific assistance, please let us know in advance to enable to assist in making your stay at the conference a pleasant and comfortable one.
General Information

Complaints
While we hope that your time at the conference is enjoyable, if you encounter a problem during your stay, please report it to the registration desk as soon as possible. The conference team will make every effort to solve the issue.
The aim of ESSDERC and ESSCIRC is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The increasing level of integration for system-on-chip design made available by advances in silicon technology is, more than ever before, calling for a deeper interaction among technologists, device experts, IC designers, and system designers. While keeping separate Technical Program Committees, ESSCIRC and ESSDERC are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions, regardless to which conference they belong.

**ESSDERC 2015 main topics**

**CMOS Processes, Devices and Integration**
CMOS scaling, Novel MOS device architectures; Circuit/device interaction and co-optimization; High-mobility channel devices; CMOS front-end or back-end processes; Interconnects; Integration of RF or photonic devices; 3D integration.

**Opto-, Power- and Microwave Devices**
New device or process architectures; New phenomena and performance improvement of optoelectronic, high voltage, smart power, IGBT, microwave devices; Passive devices, antennas and filters (including Si, Ge, SiC, GaN); Optoelectronic devices including sensors, LEDs, semiconductor lasers; Photovoltaic devices; Studies of high temperature operation; IC cooling and packaging aspects.
Conference Overview

Modeling & Simulation
Numerical, analytical and statistical modeling and simulation of electronic, optical or hybrid devices, the interconnect, isolation and 2D or 3D integration; Aspects of materials, fabrication processes and devices e.g. advanced physical phenomena (quantum mechanical and non-stationary transport phenomena, ballistic transport, ...); Compact circuit modeling; Mechanical or electro-thermal modeling and simulation; DfM.

Characterization, Reliability & Yield
Front-end and back-end manufacturing processes; 3D integration and wafer-level packaging; Reliability of materials, processes and devices; Advanced interconnects; ESD, latch-up, soft errors, noise and mismatch behavior, hot carrier effects, bias temperature instabilities, and EMI; Defect monitoring and control; Metrology; Test structures and methodologies; Manufacturing yield modeling, analysis and testing.

Advanced & Emerging Memories
Novel memory cell concepts and architectures; Embedded and stand-alone memories; DRAM, FeRAM, MRAM, PCM, CB RAM, Flash, SONOS, nanocrystal memories; single and few electron memories; 3D systems integration; Organic memories; NEMS-based devices.

MEMS, Sensors & Display Technologies
Design, fabrication, modeling, reliability, packaging and smart systems integration of actuators (discrete SoC, SiP, or heterogenous 3D integration); MEMS, NEMS, optical, chemical or biological sensors; Display technologies; High-speed imagers; TFTs; Organic and flexible substrate electronics.
Emerging Non-CMOS Devices & Technologies
Novel non-CMOS materials, processes and devices, (nanotubes, nanowires and nanoparticles, including carbon, graphene, metal oxides, ...) for electronic, optoelectronic, sensor & actuator applications; Molecular and quantum devices; Nanophotonics, plasmonics, spintronics, self-assembling methods; Energy harvesters; High frequency digital and analog devices including THz; New high-mobility channels (strained Si, Ge, SiGe).
Autonomous Driving: Requirements on Automotive Radar-Sensors

Jürgen Dickmann, Daimler AG

Automotive Radar has already found its way into nearly all car manufacturers portfolio, even for small car platforms. Up to now, the performance requirements increased steadily from simple detector tasks in blind spot monitoring systems to multipurpose sensors enabling complex driver assistance systems. The utmost push in performance requirement is initiated with the trend towards autonomous, driver less driving. Future automotive radar systems have to provide imaging like capabilities and have to interact in radar networks, which allow for highly comprehensive perception tasks. The talk will provide an overview on state of the art automotive radar usage on the basis of the DAIMLER car platforms; will give an outline on future automotive radars based on requirements for autonomous driving.

Jürgen Dickmann received his Diploma degree in electrical engineering from University Duisburg, Germany, in 1984. He obtained his Dr.-Ing. degree in 1991 from the Rheinisch Westfälische Technische Hochschule Aachen (RWTH), Germany. Beginning in 1986 he was with the AEG Research Center, where he did research on III/V-semiconductor processing techniques, mmWave devices and MMICs. Since 1990 he has been with Daimler AG, Group Research and Advanced Engineering, where he is responsible for active sensors. In addition he is also responsible for the transfer of all environmental sensing and localization activities for the new S-Class model.
Car of the Future - Electrification and Energy Management

Patrick Leteinturier, Infineon Technologies, Fellow Automotive Systems

The regulation for CO₂ reduction, pollutant reduction (CO, NOx, HC, PM...) have pushed the automotive industry for more electrification. The internal combustion engines will continue to power our vehicles for decades but will be assisted by electric traction in various xEV architectures. The race for efficiency, environment friendly, and safety will not end here. Automated and autonomous driving are opening a new field of benefits, but also a new field of challenges. The engineers will have to reinvent the EE vehicle architecture for new domain control and fail operational systems. The cars will be connected to other cars and the infrastructure with software update over the air. The new vehicles will be real cyber physical systems. This keynote will explore the potential of electronic technologies to solve the new requirements in sensing, controlling, powering, energizing the car of the future.

Patrick Leteinturier has 26 years of experience in automotive electronics. He started his career working at Lucas (UK) and SAGEM (France) developing powertrain electronic systems for PSA and Renault. He is working since 1997 at Infineon Technologies AG (Germany). He is currently responsible for system architecture of silicon products (silicon sensors, microcontrollers, silicon smart powers, and power modules) for Engine, Transmission and xEV applications.

A member of SAE International since 1998, Mr. Leteinturier received the SAE International Forest R. McFarland Award (2008). In 2010, he was named an SAE International Fellow. Mr. Leteinturier is currently SAE
director and member of the Engineering Meeting Board. In addition, Mr. Leteinturier is Guest Professor at the Tianjin University in China (since 2006).

Mr. Leteinturier received his Mechanical Engineering degree from ENSAM: Ecole Nationale Supérieure des Arts et Métiers (France) in 1987, his Master of Advanced Studies in Internal Combustion Engines (DEA) at the University Paris 6 (France), and his Electric & Electronic Engineering degree from ESE: Ecole Supérieure d’Electricité (France) in 1990.
Analog Design Challenges in Future Nanometer CMOS Technologies

Willy Sansen, KU Leuven

Important applications, such as mobile SoC, Internet of things, automotive, biomedical, etc. all require mixed-signal design and more digitally assisted analog. This presentation gives a projection on how analog design can benefit from future Nanometer CMOS technologies. Optimum biasing for minimum power consumption has to be revisioned, leading to lower supply voltages. Moreover offset and 1/f noise have to be reduced. Speed can be enhanced by inclusion of negative resistances and capacitances. Nowadays both FinFETs and FD-SOI, compete for future Nanometer design projects. Beyond gate lengths of 10 nm, more exotic materials as Germanium need to be considered however.

Willy Sansen received a PhD degree from U.C. Berkeley in 1972. Since 1980 he has been full professor at the Catholic University of Leuven, in Belgium. From 1984 to 2008, he has headed the ESAT-MICAS laboratory on analog design, which has created six spinoffs in the last fifteen years. He has been supervisor of sixty-four PhD theses and has authored and coauthored more than 650 publications and fifteen books among which the Powerpoint slide based book “Analog Design Essentials” (Springer 2006). He has been involved in several spinoffs of the KULeuven.

He is a member of several editorial and program committees of journals and conferences. He was Program Chair of the ISSCC-2002 conference and President of the IEEE Solid-State Circuits Society in 2008-2009. He is the recipient of the D.O.Pederson award of the IEEE Solid-State Circuits Society in 2011. He is a Life Fellow of the IEEE.
European Microelectronics – Leading in Automotive?

After the conference opening has started with three invited presentations:

- *Autonomous Driving: Requirements on Automotive Radar-Sensors*
  Jürgen Dickmann,
  Head of R&D Active Sensors, Daimler AG

- *Car of the Future - Electrification and Energy Management*
  Patrick Leteinturier, Fellow Automotive Systems, Infineon Technologies

- *Analog Design Challenges in Future Nanometer CMOS Technologies*
  Willy Sansen, Prof. Em., ESAT-MICAS, KU Leuven

on topics related to automotive integrated circuits and nanoscale analog and mixed signal circuits, a panel discussion will be started. Based on the fact that Europe is very active in the area of automotive electronics (chips, modules and systems) “European Microelectronics – Leading in Automotive?” has been selected as obvious title in order to challenge this throughout the panel discussion with contributions from the audience in a later phase. Besides the presenters of the three invited speeches, representatives of semiconductor companies active in automotive electronics will be at the panel:

Wolfgang Schelter, CEO, AVL Software and Functions GmbH, Germany / Kirk Laney, CEO, ams AG, Austria / Volker Graeger, CEO, NXP Semiconductors Austria GmbH / Laurent Malier, Directeur R&D, STMicroelectronics, France.

The panel will be moderated by Andreia Cathelin, STMicroelectronics, France and Wolfgang Pribyl, JOANNEUM RESEARCH, Austria.
5G Wireless Communication Beyond 2020

Jonas Hansryd, Ericsson Research

In the last twenty years we have seen a revolution comparable to the industrialization. We have gone from voice, to data, to mobile broadband to a situation where half of the two-year olds in Sweden use internet. We have changed how we are creating and sharing knowledge, how we interact with family and friends, how we work and how we do business. We have seen traditional industries transform... music, media ... and how more and more industries are rapidly digitalizing and mobilizing – realizing the need for good ICT solutions where mobility is becoming not only an opportunity, but a necessity.

Today we see more than 7.1 billion mobile subscribers which by 2020 is expected to rise to more than 9.2 billion, i.e. more than one subscription per living human. In the same timeframe the mobile data traffic, driven by video streaming, is foreseen to increase by a factor of eight. The majority of the subscribers 2020 will use 3G-WCDMA or 4G-LTE but there will also remain a large share of 2G-EDGE-only subscriptions due to cost of hardware and subscription.

Historically the capabilities of the mobile network have dictated the services provided by a network operator. What we see is changing today is that the requirements on the network come from devices and consumers, from over-the-top applications and industries and from innovative non-operator service providers utilizing the network capabilities provided by the operator. In a sense we have reached an inflection point and we are rapidly moving into a networked society whose requirements we need to fulfill with the fifth generation (5G) radio access networks.
Joint Plenary Talks

Jonas Hansryd joined Ericsson Research in 2008 and is currently managing the microwave high-speed and electronics group. He holds a Ph.D. in electrical engineering from the Chalmers University of Technology, Gothenburg, Sweden and was a visiting researcher at Cornell University, Ithaca, US, from 2003-2004.

Theoretical Analyses and Modeling for Nanoelectronics

Giorgio Baccarani, University of Bologna

In this plenary talk will be shortly discussed the evolution of Microelectronics into Nanoelectronics, according to the predictions of Moore’s law, and some of the issues related with this evolution. Next, will be addressed the requirements of device modeling related with an extreme device miniaturization, such as the band splitting into multiple subbands and quasi-ballistic transport. Physical models are summarized and a few simulation results of heterojunction TFETs are reported and discussed.

Giorgio Baccarani received the Electrical Engineering degree in 1967 and the Physics degree in 1969 from the University of Bologna. Associate Professor in Quantum Electronics since 1972 and full Professor in Electronics since 1980, he is currently Alma Mater Professor and is in charge of the course of Nanoelectronics.
Nature as Microelectronic Fab – Bioelectronics: Materials, Transistors and First Simple Circuits

Barbara Stadlober, JOANNEUM RESEARCH

Over the last five years, a series of novel organic materials that either occur freely or are extracted from nature have been applied in transistors and simple electronic circuits (inverters) as biocompatible and biodegradable dielectrics and semiconductors. Although these materials have natural origin, are abundant on earth and in many respects were exploited by humanity since centuries or even millennia, they often do not deliver the expected outcome for high performance electronics. This situation motivated chemists to synthesize organic materials inspired by the natural ones (i.e. nature-inspired), with improved structures for high-performance organic electronics development. This talk elaborates on the usage of the new class of naturally-occurring and nature-inspired organic materials employed in electronic circuits. Such novel structures impart high performance and high stability to integrated circuits, and hold the appealing features of biocompatibility and biodegradability. They carry a huge potential for achieving the sustainability goal in electronics industry, corroborated by resource efficiency and electronic waste reduction.

Dr. Barbara Stadlober is Head of the Research Group “Micro- & Nanostructuring” at the Institute of Surface Technologies and Photonics of the JOANNEUM RESEARCH Forschungsgesellschaft mbH located in Graz/Weiz, Austria. She has a background in low temperature and solid state physics, was part of the technology development team at Infineon Technologies Austria in Villach and joined JR in 2002 for building up the
Joint Plenary Talks

group “Organic Field Effect Transistors”. Her current interests range from organic and printed electronics over R2R-nanopatterning to large-area physical sensors, biosensors and biomimicry. She is author of more than 60 peer-reviewed publications and presenter of numerous invited talks at renowned conferences.

Engineered Substrates to Address Current and Future IC Challenges

Paul Boudre, Soitec

Paul Boudre joined Soitec in 2007. He was appointed Chief Executive Officer with effect from 16 January 2015. A semiconductor-industry veteran of more than 30 years, Paul Boudre gained extensive international experience through his previous positions managing industrial operations for IBM Semiconductor, STMicroelectronics, Motorola Semiconductor, and Atmel. From 1997 to 2006, he managed European operations for KLA-Tencor, one of the world's top five semiconductor equipment manufacturers. He was subsequently appointed Vice President for both the US and Europe. Paul Boudre holds a graduate degree in chemistry from France’s Ecole Nationale Supérieure de Chimie de Toulouse.
Micro-/and Nanoelectronics and Horizon 2020
Willy van Puymbroeck,
European Commission DG Connect

Closing Session
Synchronous Advancement of Hardware and Software – Added Value for Europe?

This session has been jointly organized from ESSCIRC/ESSDERC and the ECSEL stakeholders. It serves at the same time as closing session for the conference and as an introduction session for the ECSEL stakeholders meeting, which will take place after the conference. As many people are currently discussing the importance of having all elements of the electronic value chain under control and how to best finance and fund the necessary R&D efforts, “Synchronous Advancement of Hardware and Software – Added Value for Europe?” has been chosen as topic for this session. It will start with an invited speech of Willy van Puymbroeck, DG CONNECT and continue with a panel discussion of several high level representatives from the electronics industry representing hardware, software and systems industries alike. The discussion will focus on whether all elements are vital in order to gain / keep a leading position in the global markets or if some of the value chain elements can very well be abandoned in Europe and rather be purchased in some other region of the world.
This session will be moderated by Andreas Wild, Executive Director of ECSEL.
Ge/III-V MOS Device Technologies for Low Power Integrated Systems

Shinichi Takagi, Mitsuru Takenaka

CMOS utilizing high mobility Ge/III-V channels on Si substrates is expected to be one of the promising devices for high performance and low power integrated systems in the future technology nodes, because of the enhanced carrier transport properties. In addition, Tunneling-FETs (TFETs) using Ge/III-V materials are regarded as one of the most important steep slope devices for the ultra-low power applications. This talk is about device and process technologies of Ge/III-V MOSFETs and TFETs on the Si CMOS platform. The channel formation, source/drain (S/D) formation and gate stack engineering are introduced for satisfying the device requirements. The plasma post oxidation to form GeOx interfacial layers is a key gate stack technology for Ge CMOS. Also, direct wafer bonding of ultrathin body quantum well III-V-OI channels, combined with Tri-gate structures, realizes high performance III-V nMOSFETs on Si with threshold voltage tunability.

Shinichi Takagi was born in Tokyo, Japan. He received the B.S., M.S., and PhD. Degrees in electronic engineering from the University of Tokyo, Japan in 1982, 1984 and 1987, respectively. His PhD thesis involved the study on the surface carrier transport in MISFETs based on III-V semiconductors. He joined the Toshiba Research and Development Center, Kawasaki, Japan in 1987, where he has been engaged in the research on the device physics of Si MOSFETs, including the carrier transport in the inversion layer, the impact ionization phenomena, the hot carrier degradation the electric properties of Si/SiO2 interface. From 1993 to 1995, he was a Visiting Scholar at Stanford University, CA, where he studied the Si/SiGe
hetero-structure devices. In 2003 he joined the University of Tokyo, where he is currently working as a professor in the department of Electrical Engineering and Information Systems, School of Engineering. He has published more than 210 papers with high originality and has presented more than 430 papers in prestigious international conferences including more than 110 invited talks and lectures.

Investigations of Vapor Phase Deposited Transition Metal Dichalcogenide Films for Future Electronic Applications
Georg Duesberg, Trinity College Dublin

This talk presents the investigations on ultrathin and monolayered transition metal dichalcogenides (TMDs). These recently have raised much interest for their applications in electronics. TMDs can be n- and p-type semiconductors and some of them undergo a change in band structure when thinned to a monolayer. In particular, with the TMD MoS2, a number of devices such as transistors, photodiodes, LEDs and chemical sensors have been demonstrated. In this report we focus on devices derived from MoS2 that is grown by methods that can be employed for the large scale synthesis.

Prof Georg Duesberg graduated in Physical Chemistry from the University of Kassel, Germany. He worked at the Max-Planck-Institute Stuttgart and Trinity College Dublin from 1997 – 2001. He was the first person to characterise individual carbon nanotubes by Raman spectroscopy. He received his PhD from the University of Tübingen, Germany in 2000. From 2001 – 2005 he worked at the Infineon AG, Corporate Research Department, Munich, Germany. From 2005 – 2007 Prof...
Duesberg worked in the Thin Films Department of the Qimonda AG, Dresden, Germany on the implementation of new carbon nanostructured films into future DRAM technology. In July 2007 he moved to Ireland to take on a position as a Principal Investigator in CRANN and Associate Professor at Trinity College Dublin. He was made Professor and Director of Research in the School of Chemistry in July of 2011.

High Performance NEMS Devices for Sensing Applications

Thomas Ernst, CEA-Leti

NEMS based sensors open several opportunities for integrated solutions in emerging domains as chemical analysis and life science. With critical dimensions ranging between 10 and 100 nm, those devices can be made at the VLSI scale, possibly cointegrated with CMOS and are well suited for autonomous, highly sensitive or dense sensors. Several applications will be presented, as complex gas portable recognitions systems, mass spectrometry, or bio-sensors.

Thomas Ernst received his Ph.D. degrees from the National Polytechnics Institute of Grenoble, France, in 2000. From 1997 to 2000, he developed advanced SOI CMOS electrical characterization, simulation and modeling methods at STMicroelectronics and IMEP laboratory. He then joined CEA-LETI to develop novel strained-channel CMOS architectures for 32 nm technology. In particular, he was leading strained SOI, strained Germanium, and SiGeOI CMOS integration at LETI. Since 2005, he is leading the 3D multi-channels and nanowire CMOS devices developments. His expertise is in the area of novel CMOS
device fabrication technology and MOSFETs analytical modeling for electrical characterization. Dr. Ernst is author or co-author of over 130 technical journal papers and communications at international conferences on CMOS device integration, modeling and characterization. He is author or co-author of more than 15 patents. He is a member of ESSDERC and ULIS conferences technical committees since 2005 and member of IEDM TPC for 2 years. He is a recipient of research grant from the European Research Council to develop multi-physics integrated systems.
The tutorials will take place at the Messe Congress Graz.
Monday, September 14, 2015

GaN Based Power Electronics
Organizer: Oliver Häberlen, Infineon Technologies Austria

This tutorial aims at providing a broad overview on the merits and challenges of GaN based power electronics. Increasingly efficient systems to produce, distribute and use energy will be necessary to cover worldwide growing energy needs. Good news is that about a third of the global energy use is based on electricity, where power electronics will enable further significant reduction in power losses. Silicon power technology has developed tremendously over the past decades and will continue to improve. However, for highest performance levels new semiconductor materials like gallium nitride offer record figure-of-merit values compared to state-of-the-art silicon technology.

The tutorial will start with an introductive talk on a very wide-spread power electronics system, the switched mode power supply. It will show the system perspective and explain the key levers to improve the power conversion efficiency including the requirements and challenges for the power devices. It will be shown how GaN power devices enable new topologies that could not be addressed with silicon devices. The next talk will give an overview on GaN technology and device design including the basic operation principle of a GaN HEMT (2DEG and hetero structure, basic device function, HEMT, lateral device, design, normally-on vs. normally-off). The third talk will focus on the challenges of the hetero-epitaxial growth of GaN on silicon wafers to avoid the prohibitive
cost of GaN bulk substrates. Finally, since the missing full proof of reliability has hindered the new material system from entering the market the past few years, the fourth talk will give an overview over the material and device specific failure types and degradation modes.

**Agenda:**

10:50 **Switched Mode Power Supplies: System Solutions and Challenges for Power Devices**  
Gerald Deboy, Infineon Technologies Austria AG, Villach (Austria)

12:30 **Lunch**

13:30 **GaN Power Switching Transistors: Survey on Device Concepts and Technology**  
Joachim Würfl, Ferdinand-Braun-Institut für Höchstfrequenztechnik, Berlin (Germany)

15:00 **Coffee Break**

15:30 **The Material Challenge: Hetero-Epitaxial Growth of GaN on Silicon Wafers**  
Marianne Germain, EpiGaN, Hasselt (Belgium)

16:30 **Dispersion Effects, Failure Modes and Mechanisms of GaN-on-Si HEMTs for Power Electronics Applications**  
Enrico Zanoni, University of Padova, Padova (Italy)
Novel Transistors – Beyond the Planar Silicon MOSFET
Organizer: Max Lemme, University of Siegen, Germany

The aim of this tutorial is to present – in a didactic format – novel and emerging transistor options for More Moore and More Than Moore applications. Even though industry is approaching the end of physical gate length scaling, the quest for new transistor designs and materials is far from over. In fact, the options for future transistors appear to be as wide as or wider than they have ever been. The speakers of this tutorial have been carefully chosen to reflect the multitude of approaches pursued in research and development today. The target audience is PhD students with various backgrounds and industry engineers, but also aims to peak the interest researchers working in related fields. The presentations will provide a thorough introduction to the respective topics and aim to give an outlook on circuit design implications. The latter is intended to also address attendants of the sister conference, the European Solid-State Circuits Conference (ESSCIRC).

Agenda:

13:00  Thin Channel Silicon Transistors
       Geert Eneman, IMEC, Leuven (Belgium)

14:00  Coffee Break

14:30  Tunnel FETs
       Joachim Knoch, RWTH-Aachen, Aachen (Germany)

15:30  Compound Semiconductor Devices
       Suman Datta, Penn State, State College (USA)
16:30  *Coffee Break*

17:00  **2D Channel Devices**
Jörg Appenzeller, Purdue, West Lafayette (USA)

18:00  **Graphene FET Models for Circuit Design**
Sebastien Fregonese, Univ. Bordeaux, Bordeaux (France)
A Workshop Day will be organized on Friday, 18 September, 2015 and will take place at the Graz University of Technology, Campus Inffeldgasse (Entrance Inffeldgasse 25D).

MOS-AK: Enabling Compact Modeling R&D Exchange
Organizer: Wladek Grabinski, MOS-AK (EU)

The specific workshop goal will be to classify the most important directions for the future development of the electron device models, not limiting the discussion to compact models, but including physical, analytical and numerical models, to clearly identify areas that need further research and possible contact points between the different modeling domains. This workshop is designed for device process engineers (CMOS, SOI, BiCMOS, SiGe) who are interested in device modeling; ICs designers (RF/Analog/Mixed-Signal/SoC) and those starting in that area as well as device characterization, modeling and parameter extraction engineers. The content will be beneficial for anyone who needs to learn what is really behind the IC simulation in modern device models.

Agenda:
09:00   Morning MOS-AK Session
11:00   CM Standardization Panel
12:00   Lunch
13:00   Afternoon MOS-AK Session
16:00   End of Workshop
SINANO Workshop:
New Materials for Nanoelectronics
Organizer: Enrico Sangiorgi, University of Bologna

This Workshop is supported by the European Institute of Nanoelectronics SINANO (www.sinano.eu) and aims at discussing state-of-the-art results and disruptive achievements in the field of New Materials for Nanoelectronics. The integration of new materials (e.g. III-V compound semiconductors) on silicon platforms is foreseen as the next major evolution of advanced CMOS technology nodes. The introduction of such a disruptive innovation is a long term process where complex technological experiments must be matched by accurate Technology Computer Aided Design (TCAD) in order to reduce cost and to explore in a timely manner the available engineering options.

In this workshop, leading experts in the field will report on the most recent results in fabrication, characterization and modelling of nanoelectronic devices based on new materials. Workshop highlights include a demonstration and hands-on tutorial of atomic-scale simulation that will give the audience the possibility of running examples on their own computers.

Agenda:

8:45  Introduction
Enrico Sangiorgi, SiNANO Institute

9:00  Integration of III-V Devices on a Si Platform
Nadine Collaert, IMEC
### ESSDERC Workshops

<table>
<thead>
<tr>
<th>Time</th>
<th>Session</th>
<th>Speaker(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>9:40</td>
<td><strong>TCAD Device Simulation Frame for III-V MOS Device, Synopsys Representatives</strong></td>
<td>Axel Erlebach, Fabian Bufler and Martin Frey, SYNOPSYS</td>
</tr>
<tr>
<td>10:20</td>
<td><strong>III-V Heterostructures and Transition Metal Dichalcogenides for Tunnel-FETs</strong></td>
<td>Marco Pala, IMEP-LAHC, Grenoble INP, NRS</td>
</tr>
<tr>
<td>11:00</td>
<td><strong>Coffee Break</strong></td>
<td></td>
</tr>
<tr>
<td>11:30</td>
<td><strong>Graphene and Two-Dimensional (2D) Materials for Nanoelectronics</strong></td>
<td>Vikram Passi, University of Siegen</td>
</tr>
<tr>
<td>12:00</td>
<td><strong>Investigating the High-k/InGaAs MOS System for Future Logic Applications</strong></td>
<td>Paul Hurley, Tyndall</td>
</tr>
<tr>
<td>12:30</td>
<td><strong>Lunch</strong></td>
<td></td>
</tr>
<tr>
<td>13:45</td>
<td><strong>Demonstration and Hands-on Tutorial of Atomic-Scale Simulation with ATK</strong></td>
<td>Troels Markussen, Umberto Pozzoni, QuantumWise</td>
</tr>
<tr>
<td>16:00</td>
<td><strong>Coffee Break and End of Workshop</strong></td>
<td></td>
</tr>
</tbody>
</table>
RFID Technologies Exploiting 2D and 3D Printing and Packaging Techniques

Organizer:
Jasmin Grosinger, Graz University of Technology

Radio frequency identification (RFID) is a technology that offers the possibility of reading or changing data through radio waves without the need for contact. This allows the automatic identification and location of objects and makes the collection of data easier and covers a diverse application range. Styrian RFID companies – mostly situated around Graz – are highly renowned in the field of RFID technologies: more than 50% of RFID chips in use worldwide have been developed in Styria. In future developments, RFID transponder (tag) realizations will exploit the capabilities of 2D and 3D printing and packaging technologies such as the inkjet printing and embedded wafer-level ball grid array (eWLB) packaging technologies. This workshop will cope with this development and will give the workshop participants insight into recent developments in these areas.

Agenda:

08:45 Welcome and Presentation of the RFID Hotspot in Graz/Styria
Wolfgang Bösch, Graz University of Technology

09:20 Presentation and Discussion “RFID Technologies Exploiting 2D and 3D Printing and Packaging Techniques”
Jasmin Grosinger, Graz University of Technology
10:10  **Presentation and Discussion**  
“Printed Electronics – Materials, Processes and Innovative Applications”  
Andreas Klug, NanoTec Center

11:00  *Coffee break*

11:30  **Presentation and Discussion**  
“Advances in Packaging for RF Applications”  
Klaus Pressel, Infineon Technologies

12:20  **Final Discussion**

12:30  *End of Workshop*
From Atom to Transistor – Models and Techniques for Predictive Simulation of Emerging Devices

Organizer: Zlatan Stanojević, Global TCAD Solutions GmbH

50 years since the inception of Moore's Law, industry is facing ever increasing hurdles on the roadmap to produce devices which perform better and consume less power. The challenges concerning introduction of new technology nodes pose a great risk to manufacturers, and there is always more than one possible way to proceed. This workshop will discuss modern models and techniques in semiconductor device simulation. It will demonstrate and highlight the level of detail which can be included in device simulation today. A methodological hierarchy, ranging from atomistic models up to extraction of device parameters, will be presented which consistently yields results well-founded in physics. Emerging device concepts will be covered, demonstrating how the chosen approach can help assess the risks involved in the introduction of new technologies.

Agenda:

14:00 Extracting Materials Properties for Semiconductor Device Simulation from Ab-Initio and Atomistic Simulation
Erich Wimmer, Materials Design s.a.r.l. (France)

14:30 Blessing or Curse: Dissipative Quantum Transport in Nano-Scale Devices
Hans Kosina, Vienna University of Technology, Institute for Microelectronics
15:00  **Just enough Quantum – Combining Semi-classical and Quantummechanical Models for Fast and Predictive Device Simulation**  
Zlatan Stanojević, Global TCAD Solutions GmbH

15:30  **Modeling Reliability under Variability in Nano-Scale Devices**  
Ben Kaczer, IMEC (Belgium)

16:00  **Coffee Break**

16:30  **Predictive Simulation in Action: Selected Case Studies — Live Demonstration**  
Zlatan Stanojević, Erich Wimmer

17:30  **End of Workshop**
Variation-Aware Design for RF Engineers

Organizer: Stephan Weber, Cadence Design Systems

Creating an RF design is always a challenge, but producing it with acceptable yield is even more difficult. We start with discussing Monte-Carlo and PVT corner analysis, and their measures and problems like confidence intervals, uncertainties from non-normal distributions, etc. Then moving over to advanced techniques for yield prediction and optimization. A demo will be given using Cadence Virtuoso ADE GXL for design of RF key blocks.

Agenda:

8:45 Important Statistical Techniques for Circuit Design
Demonstration: Normal & Non-Normal Data Analysis, Confidence Intervals, Yield Estimation Methods, etc.

11:00 Coffee Break

11:30 Advanced Methods and Over-All Flow
Demonstration: Variation-Aware Design in Cadence Flow

12:30 End of Workshop
Electromagnetic Compatibility of Integrated Circuits
Organizer: Bernd Deutschmann, Gunter Winkler, Graz University of Technology

Today very complex electronic systems often consisting of large digital cores, analog and mixed-signal circuits, as well as power electronic devices can be realized in one single chip. But, as device dimensions are shrinking, ICs are often becoming more susceptible to electromagnetic interferences; on the other hand internal switching frequencies of modern ICs increasing, resulting in higher electromagnetic emission. Therefore, the design of ICs that are compliant to electromagnetic compatibility (EMC) specifications has become more and more challenging during the last years. Noise signals such as radio-frequency interferences or transient disturbances such as electrostatic discharges (ESD) can interfere with the operation of the ICs and particularly with the analog circuits embedded in such devices. The undisturbed operation of electronic systems is of vital importance for safety and reliability and should therefore be of particular concern for designers of integrated circuits. In the first part of this workshop an introduction to EMC at the IC level as well as an overview of the most important EMC measurement techniques that are used for the characterization of the emission and immunity of ICs are given. In the further parts carefully selected IC design related topics such as the susceptibility to electromagnetic interferences of sensor signal conditioning circuits, the influences of packaging, connectors, PCB traces and ground planes on the performance of ICs with respect to EMC, as well as on-chip decoupling to improve the EMC of ICs will be presented.
Agenda:

14:00  Introduction to EMC at the IC Level, EMC Measurement Techniques of ICs
       Bernd Deutschmann, Gunter Winkler

14:40  Susceptibility to EMI of Sensor Signal Conditioning Circuits
       Franco Fiori

15:20  Influence of Packaging, Connectors, PCB Traces and Ground Plane on the Performance of ICs with Respect to EMC
       Adrijan Baric

16:00  Coffee Break

16:30  Pro and Cons of Onchip Decoupling to Improve the EMC of Integrated Circuits
       Timm Ostermann

17:30  End of Workshop
Variability – From Equipment to Circuit Level
Organizer: Jürgen Lorenz, Fraunhofer IISB

This workshop deals with process variability which is one of the key physical limitations which challenge progress in nanoelectronics. Effects from various sources of process variations, both systematic and stochastic, influence each other and lead to variations of the electrical, thermal and mechanical behavior of devices, interconnects and circuits. Correlations are of key importance because they drastically affect the percentage of products which meet the specifications. Whereas the comprehensive experimental investigation of these effects is largely impossible, modelling and simulation (TCAD) offers the unique possibility to predefine process variations and trace their effects on subsequent process steps and on devices and circuits fabricated, just by changing the corresponding input data. This important requirement for and capability of simulation is among others highlighted in the International Technology Roadmap for Semiconductors ITRS.

In view of this in the FP7 project SUPERTHEME a software system has been developed which enables the simultaneous assessment of the impact of systematic variations caused by process equipment and statistical variations caused by the granularity of matter on advanced More Moore and More than Moore devices and circuits. Within this workshop variability challenges will be outlined, and a selection of results obtained in SUPERTHEME will be presented. Furthermore, it is planned to also introduce related projects which are complementary to SUPERTHEME.
Agenda:

8:45  Welcome and Orientation
      Jürgen Lorenz, Fraunhofer IISB

9:00  Variability at all Levels – A Challenge for the
      Semiconductor Industry
      Andre Juge, ST

9:30  Overview of the SUPERTHEME Project
      Jürgen Lorenz, Fraunhofer IISB

10:00 Defects Responsible for BTI in CMOS Devices:
      MORDRED Perspective
      Alexander Shluger, UCL

10:30 Variability Aware Process Simulation in
      SUPERTHEME
      Eberhard Bär, Fraunhofer IISB

11:00 Coffee Break

11:30 Variability Aware Process Simulation in
      SUPERTHEME
      Asen Asenov, GU/GSS

12:00 Hierarchical Modeling of Reliability and Time
      Dependent Variability in the MORV Project
      Ben Kaczer, IMEC

12:30 Lunch

14:00 Covering Variability from Unit Process up to
      Circuit Level for Mixed – Signal Circuits
      Rainer Minixhofer, ams
14:30  Variability Aware SPICE Modeling and Circuit Simulation in SUPERTHEME
       Campbell Millar, GSS

15:00  Open Discussion and Concluding Remarks

15:30  End of Workshop
DC-DC Converter Techniques
Organizer: Christoph Sandner, Infineon Technologies

This workshop will give insights into different key aspects of DC-DC converter concept and design. The designated speakers are worldwide recognized experts in this field. We target one speech in each of these fields: Inductor based converters, switched capacitor converter concepts and control techniques, buck converter control and stability, and last not least a talk about how to avoid most common mistakes in DC-DC converter circuit design.

**Agenda:**

8:30  **Switched Capacitor DC-DC Converters: Concepts and Control Techniques**
Hans Meyvaert, KU Leuven, Belgium

9:30  **Inductor Based DC-DC Converters**
tba

10:30  **Coffee Break**

11:00  **Ripple-Based Control Techniques for Buck Type DC-DC Converters**
Jesus A. Oliver, UPM Madrid, Spain

12:00  **How to Avoid Most Common Mistakes in DCDC Design: Voltage Mode, PWM and fixed Frequency**
Vadim Ivanov, TI, USA

13:00  **End of Workshop**
Tuesday, September 15

A0L-A JOINT PLENARY: J. Dickmann / P. Leteinturier ........ 79
A1L-A JOINT PLENARY: Willy Sansen .................................. 79
A3L-D Compact Models ................................................. 80
A3L-E Technology, Design and Characterization of Wide Bandgap Power Devices ................. 81
A3L-F FOCUS SESSION: FDSOI part 1 ............................... 82
A5L-D ESSDERC Plenary: S. Takagi .................................. 83
A7L-D Emerging Devices & Technologies I ....................... 84
A7L-E Nonvolatile Memory Technologies ......................... 85
A7L-F Innovative Approaches for Opto and Power Devices .................................................................. 86

Wednesday, September 16

B1L-A JOINT PLENARY: J. Hansryd / G. Baccarani ............ 87
B2L-E MEMS and Sensors .................................................. 88
B2L-F FOCUS SESSION: FDSOI part 2 ............................... 89
B3L-E 2D Devices ............................................................. 90
B3L-F FOCUS SESSION: Yield and Manufacturing .......... 91
B4L-D ESSDERC Plenary - G. Duesberg ......................... 92
B5L-E Sensor Systems ....................................................... 93
B6L-D Emerging Devices & Technologies II .................... 94
B6L-F Reliability and Variability ....................................... 95

Thursday, September 17

C1L-A JOINT PLENARY: B. Stadlober / P. Boudre ................ 96
ESSDERC Technical Program

C2L-D  Modeling of Important Issues for Main Stream Silicon Devices ......................................................... 97

C2L-E  Advanced CMOS Device and Technology ............ 98

C2L-F  Resistive RAM ........................................... 99

C2L-G  Invited Session: Sensors and MEMS Applications ............................................................. 100

C3L-D  ESSDERC Plenary - T. Ernst ......................... 101

C4L-C  Invited Session: Advanced Biomedical Devices ... 102

C4L-E  Characterization of Advanced Devices .............. 103

C4L-F  Advanced Numerical Modeling of Alternative Material Devices ............................................... 104
Tuesday, September 15

JOINT PLENARY: J. Dickmann / P. Leteinturier
Session Code: A0L-A
Location: Graz
Time: 09:00 - 10:20
Chair(s): Franz Dielacher; Infineon
Martin Schrems; ams AG

09:00 Autonomous Driving: Requirements on Automotive Radar-Sensors
Jürgen Dickmann
Daimler AG, Germany

09:40 Car of the future Electrification and Energy Management
Patrick Leteinturier
Infineon Technologies AG, Germany

JOINT PLENARY: Willy Sansen
Session Code: A1L-A
Location: Graz
Time: 10:40 - 11:20
Chair(s): Franz Dielacher; Infineon
Martin Schrems; ams AG

10:40 Analog Design Challenges in future Nanometer CMOS Technologies
Willy Sansen
European Commission DG Connect, Belgium
Tuesday, September 15

Compact Models

Session Code: A3L-D
Location: Salzburg
Chair(s): Wladek Grabinski; Cristell Maneux; IMS Bordeaux

Mark Lundstrom
Purdue University, United States

14:00 Compact Modeling of DG-Tunnel FET for Verilog-A Implementation
Arnab Biswas¹, Luca De Michielis², Antonios Bazigos¹, Adrian Mihai Ionescu¹
¹Ecole Polytechnique Fédérale de Lausanne, Switzerland; ²Independent Contractor, Switzerland

14:20 Modeling of the Conduction Characteristics of Voltage-Driven Bipolar RRAMs Including Turning Point Effects
Juli Blasco, Jordi Suñé, Enrique Miranda
Universitat Autonoma de Barcelona, Spain

14:40 A Surface Potential and Current Model for Polarity-Controllable Silicon Nanowire FETs
Jian Zhang, Pierre-Emmanuel Gaillardon, Giovanni De Micheli
École Polytechnique Fédérale de Lausanne, Switzerland

15:00 Mixed-Domain Compact Modeling Framework for Fluid Flow Driven by Electrostatic Organic Actuators
Hiroshima University, Japan
Tuesday, September 15

Technology, Design and Characterization of Wide Bandgap Power Devices

Session Code: A3L-E  
Location: Linz  
Chair(s): Gianmauro Pozzovivo; Infineon Technologies Austria  
Susanna Reggiani; Università di Bologna

13:20 Charge Trapping in Gate-Drain Access Region of AlGaN/ GaN MIS-HEMTs After Drain Stress  
Simon Jauss1, Stephan Schwaiger2, Walter Daves2, Stefan Noll1, Oliver Ambacher1  
1Fraunhofer IAF, Germany; 2Robert Bosch GmbH, Germany

13:40 E-Mode AlGaN/GaN True-MOS, with High-K ZrO2 Gate Insulator  
Mattia Capriotti2, Clément Fleury2, Ole Bethege2, Matteo Rigato2, Suzanne Lancaster2, Dionyz Pogany2, Gottfried Strasser2, Eldad Bahat-Treidel1, Oliver Hiitl1, Frank Brunner1, Joachim Würfl1  
1Ferdinand Braun Institut, Germany; 2Technische Universität Wien, Austria

14:00 (Invited) Technology and Design of GaN Power Devices  
Peter Moens, Abhishek Banerjee, P. Coppens, Aurore Constant, Piet Vanmeerbeek, Zilan Li, Frederick Declercq, Luc De Schepper, Herbert De Vleschouwer, Charlie Liu, Balaji Padmanabhan, Woochul Jeon, Jia Guo, A. Salih, M. Tack  
ON Semiconductor, Belgium

14:40 Experimental Analysis of Planar Edge Terminations for High Voltage 4H-SiC Devices  
Victor Soler2, Maxime Berthou3, Andrei Mihai1, Josep Montserrat1, Philippe Godignon2, Jose Rebollo2, Jose Millán2  
1ABB Switzerland, Switzerland; 2Institut de Microelectrònica de Barcelona / Consejo Superior de Investigaciones Científicas, Spain; 3Université de Lyon, INSA de Lyon Laboratoire Ampere CNRS, France

15:00 On the Fly Characterization of Charge Trapping Phenomena at GaN/Dielectric and GaN/AlGaN/Dielectric Interfaces Using Impedance Measurements  
Roberta Stradiotto2, Gregor Pobegen2, Clemens Ostermaier1, Tibor Grasser3  
1Infineon Technologies AG, Austria; 2KAI GmbH, Austria; 3Technische Universität Wien, Austria
Tuesday, September 15

FOCUS SESSION: FDSOI part 1

Session Code: A3L-F
Location: Innsbruck
Chair(s): Thomas Ernst; CEA-LETI

13:20 UTBB FDSOI: Evolution and Opportunities
Thomas Skolnicki, Stephane Monfray
STMicroelectronics, France

14:00 Implementation of ARM® Cores in FinFET Technologies
Yves Laplanche
ARM, France

14:40 FinFET Versus UTBB SOI - a RF Perspective
Jean-Pierre Raskin
Université Catholique de Louvain, Belgium
Tuesday, September 15

ESSDERC Plenary: S. Takagi

Session Code: A5L-D
Location: Klagenfurt
Time: 15:40 - 16:20
Chair(s): Tibor Grasser; Technische Universität Wien

15:40 Ge/III-V MOS Device Technologies for Low Power Integrated Systems
Shinichi Takagi, Mitsuru Takenaka
University of Tokyo, Japan
Emerging Devices & Technologies I

Session Code: A7L-D
Location: Salzburg
Time: 16:20 - 18:00
Chair(s): Cees De Groot; Univ. of Southampton
Elena Gnani; Università di Bologna

16:20 Antenna-Coupled Single-Metal Thermocouple Array for Energy Harvesting
Gergo Szakmany, Alexei Orlov, Gary Bernstein, Wolfgang Porod
University of Notre Dame, United States

16:40 Novel CMOS-Compatible a-Si Based Oscillator and Threshold Switch
Abhishek Sharma, Marek Skowronski, James Bain, Jeffrey Weldon
Carnegie Mellon University, United States

17:00 Modelling and Simulation of Nanomagnetic Logic with Cadence Virtuoso Using Verilog-A
Gražvydas Žiemys, Andrew Giebfried, Markus Becherer, Irina Eichwald, Doris Schmitt-Landsiedel, Stephan Breitkreutz-V. Gamm
Technische Universität München, Germany

17:20 Non-Boolean Computing Based on Linear Waves and Oscillators
Gyorgy Csaba¹, Adam Papp², Wolfgang Porod², Ramazan Yeniceri¹
¹Istanbul Technical University, Turkey; ²University of Notre Dame, United States

17:40 Plasmonic and Electronic Device Integrated Circuits and Their Characteristics
Mitsuo Fukuda, Hiroki Sakai, Takehiro Mano, Yu Kimura, Masashi Ota, Masashi Fukuhara, Takuma Aihara, Yuya Ishii, Takeshi Ishiyama
Toyohashi University of Technology, Japan
Tuesday, September 15

Nonvolatile Memory Technologies

Session Code: A7L-E
Location: Linz
Time: 16:20 - 18:00
Chair(s): Paolo Pavan; Univ. Modena & Reggio Emilia
Georg Tempel; Infineon

16:20 (Invited) Emerging Nonvolatile Memory (NVM) Technologies
An Chen
GlobalFoundries, United States

17:00 Optimization of the Write Algorithm at Low-Current (10µA) in Cu/Al2O3-Based Conductive-Bridge RAM
Attilio Belmonte¹, Andrea Fantini¹, Augusto Redolfi¹, Michel Houssa², Malgorzata Jurczak¹, Ludovic Goux¹
¹imec, Belgium; ²Katholieke Universiteit Leuven, Belgium

17:20 On the Voltage Scaling Potential of SONOS Non-Volatile Memory Transistors
Johannes Ocker³, Stefan Slesazeck³, Thomas Mikolajick⁴, Steffen Buschbeck¹, Stefan Günther¹, Ekatarina Yurchuk¹, Raik Hoffmann², Volkhard Beyer²
¹Anvo-Systems Dresden GmbH, Germany; ²Fraunhofer IPMS, Germany; ³NaMLab gGmbH, Germany; ⁴NaMLab gGmbH / Technische Universität Dresden, Germany

17:40 High Performance Low A/R Poly PN Diode for 20nm Node PCRAM Cell Switch
Young Ho Lee, Min Yong Lee, Seung Beom Baek, Jong Chul Lee, Su Jin Chae, Hae Chan Park, Byoung Ki Lee, Hyeong Soo Kim
SK Hynix Inc., Korea, South
Innovative Approaches for Opto and Power Devices

Session Code: A7L-F
Location: Innsbruck
Time: 16:20 - 18:00
Chair(s): Edwin Piner; Texas State Univ.
Dana Cristea; IMT - Bucharest

16:20 The World's First High Voltage GaN-on-Diamond Power Devices
Turar Baltynov, Vineet Unni, Shankar Narayanan Ekkanath Madathil
University of Sheffield, United Kingdom

16:40 Fabrication of High Performance AlGaN/GaN FinFET by Utilizing Anisotropic Wet Etching in TMAH Solution
Dong-Hyeok Son², Young-Woo Jo², Ryun-Hwi Kim², Chan Heo², Jae Hwa Seo², Jin Su Kim², In Man Kang², Sorin Cristoloveanu¹, Jung-Hee Lee²
¹Grenoble Polytechnic Institute / IMEP-LAHC, France; ²Kyungpook National University, Korea, South

17:00 EDMOS in Ultrathin FDSOI: Effect of Doping and Layout of the Drift Region
Antoine Litty³, Sylvie Ortolland², Dominique Golanski², Christian Dutto², Sorin Cristoloveanu¹
¹Grenoble Polytechnic Institute / IMEP-LAHC, France; ²STMicroelectronics, France; ³STMicroelectronics / IMEP-LAHC, France

17:20 Monolithically Integrated Optical Random Pulse Generator in High Voltage CMOS Technology
Abbas Khanmohammadi, Reinhard Enne, Michael Hofbauer, Horst Zimmermann
Technische Universität Wien, Austria

17:40 Energy Harvesting with on-Chip Solar Cells and Integrated DC/DC Converter
Christoph Steffan¹, Philipp Greiner¹, Bernd Deutschmann¹, Carolin Kollegger¹, Gerald Holweg²
¹Graz University of Technology, Austria; ²Infineon Technologies AG, Austria
Wednesday, September 16

JOINT PLENARY: J. Hansryd / G. Baccarani

Session Code: B1L-A
Location: Graz
Time: 08:40 - 10:00
Chair(s): Martin Schrems; ams AG
Gernot Hueber; NXP Semiconductors Austria

08:40 5G Wireless Communication Beyond 2020
Jonas Hansryd
Ericsson Research, Sweden

09:20 Theoretical Analyses and Modeling for Nanoelectronics
Giorgio Baccarani, Emanuele Baravelli, Elena Gnani, Antonio Gnudi, Susanna Reggiani
Università di Bologna, Italy
Wednesday, September 16

MEMS and Sensors

Session Code: B2L-E
Location: Linz
Time: 10:50 - 12:10
Chair(s): Piotr Grabiec; Inst. of Electron Technology
Sebastien Hentz; CEA

10:50 Compact Heterodyne NEMS Oscillator for Sensing Applications
Marc Sansa, Guillaume Gourlat, Guillaume Jourdan, Patrick Villard, Gilles Sicard, Sébastien Hentz
CEA-Leti / Université Grenoble Alpes, France

11:10 Piezoresistive Transduction Optimization of P-Doped Poly-Silicon NEMS
Issam Ouerghi, Willy Ludurczak, Laurent Duraffourg, Carine Ladner, Anouar Idrissi-El Oudrhiri, Patrice Gergaud, Maud Vinet, Thomas Ernst
CEA-Leti, France

11:30 Fast High Power Capacitive RF-MEMS Switch for X-Band Applications
Afshin Ziaei², Shailendra Bansropun², Paolo Martins², Matthieu Le Baillif¹
¹Thales Research & Technology France, France; ²Thales TRT, France

11:50 Charge Transfer Speed Analysis in Pinned Photodiode CMOS Image Sensors Based on a Pulsed Storage-Gate Method
Alice Pelamatti³, Vincent Goiffon³, Aziouz Chabane³, Pierre Magnan³, Cédric Virmontois², Olivier Saint-Pé¹, Michel Breart de Boisanger¹
¹Airbus Defence and Space, France; ²Centre National d’Etudes Spatiales, France; ³Institut Supérieur de l’Aéronautique et de l’Espace / Université de Toulouse, France
Wednesday, September 16

FOCUS SESSION: FDSOI part 2

Session Code: B2L-F
Location: Innsbruck
Time: 10:50 - 12:10
Chair(s): Thomas Ernst; CEA-LETI

10:50 Scalability of Planar FDSOI and FinFETs and What's in Store for the Future Beyond That? 
Bruce B. Doris, Terence Hook
IBM Research GmbH, United States

11:30 UTBB FDSOI Technology Flexibility for Ultra Low Power Internet-of-Things Applications
Edith Beigne, Jean-Frédéric Christmann, Alexandre Valentian, Olivier Billoint, Esteve Amat, Dominique Morche
CEA-Leti, France

Wednesday, September 16

FOCUS SESSION: Modeling for the Future and its Design Interpretation

Session Code: B2L-C
Location: Klagenfurt
Time: 10:50 - 12:10
Chair(s): Peter Mole; Intersil
Wladek Grabinski; 0

10:50 BSIM-CMG: Standard FinFET Compact Model for Advanced Circuit Design
Juan P. Duarte², Sourabh Khandelwal², Aditya Medury², Chenming Hu², Pragya Kushwaha¹, Harshit Agarwal¹, Avirup Dasgupta¹, Yogesh S. Chauhan¹
¹Indian Institute of Technology Kanpur, India; ²University of California, Berkeley, United States

11:30 Low-Power Analog/RF Circuit Design Based on the Inversion Coefficient
Christian Enz, Maria-Anna Chalkiadaki, Anurag Mangla
École Polytechnique Fédérale de Lausanne, Switzerland
Li Tao, Weinan Zhu, Joon-Seok Kim, Deji Akinwande
University of Texas at Austin, United States

14:00 Interplay Between Hot Carrier and Bias Stress Components in Single-Layer Double-Gated Graphene Field-Effect Transistors
Yury Illarionov, Michael Waltl, Anderson Smith, Sam Vaziri, Mikael Östling, Max Lemme, Tibor Grasser
1KTH Royal Institute of Technology, Sweden; 2Technische Universität Wien, Austria; 3Universität Siegen, Germany

14:20 Characterization and Modeling of Low-Frequency Noise in CVD-grown Graphene FETs
Chhandak Mukherjee, Jorge Daniel Aguirre-Morales, Sébastien Fregonese, Thomas Zimmer, Cristell Maneux, Henri Happy, Wei Wei
1Université Lille 1, France; 2University of Bordeaux, France

14:40 A New Physics-Based Compact Model for Bilayer Graphene Field-Effect Transistors
Jorge Daniel Aguirre-Morales, Sébastien Frégonèse, Chhandak Mukherjee, Cristell Maneux, Thomas Zimmer
University of Bordeaux, France

15:00 Systematic Comparison of Metal Contacts on CVD Graphene
Amit Gahoi, Vikram Passi, Satender Kataria, Stefan Wagner, Andreas Bablich, Max Lemme
Universität Siegen, Germany
Wednesday, September 16

FOCUS SESSION: Sensors and Smart Systems

Session Code: B3L-C
Location: Klagenfurt
Chair(s): Kofi Makinwa; TU Delft

13:20  FOCUS: Key Building Blocks and Integration Strategy of a Miniaturized Wireless Sensor Node
Taekwang Jang, Seokhyeon Jeong, Myungjoon Choi, Wanyeong Jung, Gyouho Kim, Yen-Po Chen, Yejoong Kim, Wootaek Lim, Dennis Sylvester, David Blaauw
University of Michigan, United States

13:40  An Integrated Fluxgate Magnetometer for Use in Closed-Loop/Open-Loop Isolated Current Sensing
Martijn Snoeij, Viola Schaffer, Sudarshan Udayashankar, Mikhail Ivanov
Texas Instruments Deutschland GmbH, Germany

14:00  A 0.02mm² Embedded Temperature Sensor with ±2°C Inaccuracy for Self-Refresh Control in 25nm Mobile DRAM
Yeomyung Kim³, Woojun Choi³, Jaehoon Kim², Sanghoon Lee², Sangho Lee², Hyeongon Kim², Kofi Makinwa¹, Youngcheol Chae³, Taewook Kim³
¹Delft University of Technology, Netherlands; ²SK Hynix Inc., Korea, South; ³Yonsei University, Korea, South

14:20  A Temperature Sensor with a 3 Sigma Inaccuracy of ±2°C Without Trimming from -50°C to 150°C in a 16nm FinFET Process
Mei-Chen Chuang, Chia-Liang Tai, Ying-Chih Hsu, Alan Roth, Eric Soenen
Taiwan Semiconductor Manufacturing Company, Limited, United States

14:40  A Ratiometric Readout Circuit for Thermal-Conductivity-Based Resistive Gas Sensors
Zeyu Cai¹, Robert van Veldhoven², Annelies Falepin², Hilco Suy², Eric Sterckx², Kofi Makinwa¹, Michiel Pertjfs¹
¹Delft University of Technology, Netherlands; ²NXP Semiconductors, Belgium
Wednesday, September 16

FOCUS SESSION: Yield and Manufacturing

Session Code: B3L-F
Location: Innsbruck
Chair(s): Martin Schellenberger; Fraunhofer IISB
Dieter Rathei; DR Yield

13:20 Yield and Complexity Considerations for Advanced Semiconductor Manufacturing
Edward Barth
SEMATECH, Germany

13:50 Knowledge management and C-K theory within the scope of the Quality & FMECA processes for production equipment variability control purpose
Stephane Hubac
ST Microelectronics, Germany

14:20 Device Level Screening – Improve Quality and Enhance Yield
Andre Kaestner
Infineon Technologies AG, Germany

14:50 Manufacturing of 3D-integrated Optoelectronic and Photonic ICs and Systems
Franz Schrank, Jochen Kraft, Martin Schrems
ams AG
15:40  Investigations of Vapor Phase Deposited Transition Metal Dichalcogenide Films for Future Electronic Applications
Toby Hallam, Hye-Young Kim, Maria O’Brien, Riley Gatensby, Niall McEvoy, Georg Duesberg
Trinity College Dublin, Ireland
Wednesday, September 16

Sensor Systems

Session Code: B5L-E
Location: Linz
Time: 16:20 - 18:00
Chair(s): Piotr Grabiec; Inst. of Electron Technology
Sebastien Hentz; CEA

16:20 (Invited) Sensors and the Internet of Things
Matthias Streiff
SENSIRION AG, Switzerland

17:00 A Multi-Functional 200,000 Lines/s Tri-Linear RGB Line-Scan Sensor
Werner Brockherde², Benjamin Bechen², Ernst Bodenstorfer¹, Jörg Brodersen¹, Konrad Mayer¹, Christian Nitta², Olaf Schrey²
¹Austrian Institute of Technology, Austria; ²Fraunhofer IMS, Germany

17:20 Unified System Level Model of Adsorption/Desorption Process and Sensing Electronics for Vapor Trace Detection of Different Molecules in the Air
Drago Strle, Janez Trontelj
University of Ljubljana, Slovenia

17:40 Concept for a Security Aware Automatic Fare Collection System Using HF/UHF Dual Band RFID Transponders
Lukas Zöschner¹, Jasmin Grosinger¹, Raphael Spreitzer¹, Ulrich Muehlmann², Hannes Gross¹, Wolfgang Bösch¹
¹Graz University of Technology, Austria; ²NXP Semiconductors, Austria
Wednesday, September 16

Emerging Devices & Technologies II

Session Code: B6L-D
Location: Salzburg
Time: 16:20 - 18:00
Chair(s): Steve Hall; Univ. of Liverpool
Ryoichi Ishihara; TU Delft

16:20 Step Tunneling-Enhanced Hot-Electron Injection in Vertical Graphene Base Transistors
Sam Vaziri², Melkamu Belete³, Anderson Smith², Eugenio Dentoni Litta², Grzegorz Lupina¹, Max Lemme³, Mikael Östling²
¹Innovations for High Performance Microelectronic, Germany; ²KTH Royal Institute of Technology, Sweden; ³Universität Siegen, Germany

16:40 Vertical Field Effect Transistor with Sub-15nm Gate-All-Around on Si Nanowire Array
Guilhem Larrieu¹, Youssouf Guerfi¹, Xiang-Lei Han², Nicolas Clément²
¹LAAS-CNRS, France; ²Université Lille 1 / IEMN-CNRS, France

17:00 Physical and Electrical Characterization of Mg-Doped ZnO Thin-Film Transistors
Andrew Shaw, Thomas Whittles, Ivona Mitrovic, Jidong Jin, Jacqueline Wrench, David Hesp, Vin Dhanak, Paul Chalker, Steve Hall
University of Liverpool, United Kingdom

17:20 Strain Effect on Mobility in Nanowire MOSFETs Down to 10nm Width: Geometrical Effects and Piezoresistive Model
Johan Pelloux-Prayer², Mikaël Cassé², François Triozon², Sylvain Barraud², Yann-Michel Niquet¹, Jean-Luc Rouvière¹, Olivier Faynot², Gilles Reimbold²
¹CEA, DSM/INAC, France; ²CEA-Leti, France

17:40 Metal Gate VT Modulation Using PLAD N2 Implants for Ge p-FinFET Applications
Shraddha Kothari², Chandan Joishi², Dhirendra Vaidya², Hasan Nejad¹, Benjamin Colombeau¹, Swaroop Ganguly², Saurabh Lodha²
¹Applied Materials Inc., United States; ²Indian Institute of Technology Bombay, India
Wednesday, September 16

Reliability and Variability

Session Code: B6L-F
Location: Innsbruck
Time: 16:20 - 18:00
Chair(s): Guido Groeseneken; IMEC
Gunnar Malm; KTH

16:20 (Invited) The Defect-Centric Perspective of Device and Circuit Reliability – from Individual Defects to Circuits
Ben Kaczer¹, Jacopo Franco¹, Pieter Weckx³, Philippe Roussel¹, Erik Bury¹, Moonju Cho¹, Robin Degraeve¹, Dimitri Linten¹, Guido Groeseneken², Halil Kukner¹, Praveen Raghavan¹, Francky Catthoor⁷, Gerhard Rzepa³, Wolfgang Goes³, Tibor Grasser³
¹imec, Belgium; ²imec / Katholieke Universiteit Leuven, Belgium; ³Technische Universität Wien, Austria

17:00 Experimental Evidences and Simulations of Trap Generation Along a Percolation Path
Louis Gerrer⁴, Razaidi Hussin⁴, Salvatore Maria Amoroso¹, Jacopo Franco³, Pieter Weckx³, Marco Simicic², Naoto Horiguchi², Ben Kaczer², Tibor Grasser³, Asen Asenov¹
¹Gold Standard Simulations Ltd, United Kingdom; ²imec, Belgium; ³Technische Universität Wien, Austria; ⁴University of Glasgow, United Kingdom

17:20 Threshold Voltage and on-Current Variability Related to Interface Traps Spatial Distribution
Vikas Velayudhan², Javier Martin-Martinez², Marc Porti², Carlos Couso², Rosana Rodriguez², Montserrat Nafria², Xavier Aymerich², Carlos Marquez¹, Francisco Gamiz¹
¹Universidad de Granada, Spain; ²Universitat Autonoma de Barcelona, Spain

17:40 Reliability Aspects of TiSi-Schottky Barrier Diodes in a SiGe BiCMOS Technology
Andreas Mai, Alexander Fox
Innovations for High Performance Microelectronic, Germany
JOINT PLENARY: B. Stadlober / P. Boudre

Session Code: C1L-A
Location: Graz
Time: 08:40 - 10:00
Chair(s): Tibor Grasser; Technische Universität Wien
Franz Dielacher; Infineon

08:40  Nature as Microelectronic Fab
Barbara Stadlober, Esther Karner, Andreas Petritz, Alexander Fian, Mihai Irimia-Vladu
Joanneum Research Forschungsgesellschaft mbH, Austria

09:20  Engineered Substrates to Address Current and Future IC Challenges
Paul Boudre
Soitec, France
Thursday, September 17

Modeling of Important Issues for Main Stream Silicon Devices

Session Code: C2L-D
Location: Salzburg
Time: 10:50 - 12:10
Chair(s): Bernd Meinerzhagen; TU Braunschweig
          An De Keersgieter; IMEC

10:50  Statistical Simulations of 6T-SRAM Cell Ageing Using a Reliability Aware Simulation Flow
Razaidi Hussin¹, Louis Gerrer³, Jie Ding³, Liping Wang³, Salvatore Maria Amoroso¹, Binjie Cheng¹, Dave Reid¹,
Pieter Weckx², Marco Simicic², Jacopo Franco², Annelies Vanderheyden², Danielle Vanhaeren², Naoto Horiguchi², Ben
Kaczcer², Asen Asenov¹
¹Gold Standard Simulations Ltd, United Kingdom; ²imec, Belgium; ³University of Glasgow, United Kingdom

11:10  Optimization of Trigate-on-Insulator MOSFET Aspect Ratio with MASTAR
Gaspard Hiblot², Quentin Rafhay¹, Loic Gaben², Gerard Ghibaudo¹, Frederic Boeuf²
¹IMEP-LAHC, France; ²STMicroelectronics, France
Thursday, September 17

Advanced CMOS Device and Technology

Session Code: C2L-E
Location: Linz
Time: 10:50 - 12:10
Chair(s): Jurriaan Schmitz; Univ. Twente
Erwin Hijzen; NXP

10:50 Effective Work Function Engineering by Sacrificial Lanthanum Diffusion on HfON-Based 14 nm NFET Devices
Carlos Suarez-Segovia\(^5\), Charles Leroux\(^1\), Florian Domengie\(^3\), Karen Dabertrand\(^3\), Vincent Joseph\(^3\), Giovanni Romano\(^4\), Pierre Caubet\(^3\), Stephane Zoli\(^3\), Olivier Weber\(^1\), Gerard Ghibaudo\(^2\), Gilles Reimbold\(^1\), Michel Haond\(^3\)
\(^1\)CEA-Leti, France; \(^2\)IMEP-LAHC, France; \(^3\)STMicroelectronics, France; \(^4\)STMicroelectronics, CEA-Leti, France; \(^5\)STMicroelectronics, CEA-Leti / IMEP-LAHC, France

11:10 Sharp-Switching Z²-FET Device in 14 nm FDSOI Technology
Hassan El Dirani\(^4\), Yohann Solaro\(^2\), Pascal Fonteneau\(^3\), Philippe Ferrari\(^2\), Sorin Cristoloveanu\(^1\)
\(^1\)Grenoble Polytechnic Institute / IMEP-LAHC, France; \(^2\)IMEP-LAHC, France; \(^3\)STMicroelectronics, France; \(^4\)STMicroelectronics / IMEP-LAHC, France

11:30 Substrate Noise Isolation Improvement by Helium-3 Ion Irradiation Technique in a Triple-Well CMOS Process
Ning Li\(^2\), Takeshi Inoue\(^1\), Takuichi Hirano\(^2\), Jian Pang\(^2\), Rui Wu\(^2\), Kenichi Okada\(^2\), Hitoshi Sakane\(^1\), Akira Matsuzawa\(^2\)
\(^1\)S.H.I.Examination & Inspection Ltd, Japan; \(^2\)Tokyo Institute of Technology, Japan

11:50 New Layout Design Methodology for Monolithically Integrated 3D CMOS Logic Circuits Based on Parasitics Engineering
Chika Tanaka, Keiji Ikeda, Masumi Saitoh
Toshiba Corporation, Japan
Thursday, September 17

Resistive RAM

Session Code: C2L-F
Location: Innsbruck
Time: 10:50 - 12:10
Chair(s): Thomas Mikolajick; NamLab
Elisa Vianello; CEA-LETI

10:50 Engineering of a TiN|Al2O3|(Hf,Al)O2|Ta2O5|Hf RRAM Cell for Fast Operation at Low Current
Chao Yang Chen2, Ludovic Goux1, Andrea Fantini1, Robin Degraeve1, Augusto Redolfi1, Guido Groeseneken2, Malgorzata Jurczak1
1imec, Belgium; 2imec / Katholieke Universiteit Leuven, Belgium

11:10 Benefit of Al2O3/HfO2 Bilayer for BEOL RRAM Integration Through 16kb Memory Cut Characterization
Mourad Azzaz2, Antoine Benoist2, Elisa Vianello1, Daniele Garbin1, Eric Jalaguier1, Carlo Cagli1, Christelle Charpin1, Sophie Bernasconi1, Simon Jeannot2, Tristan Dewolf1, Guillaume Audoit1, Cyril Guedj1, Stéphane Denorme2, Philippe Candelier2, Claire Fenouillet-Beranger1, Luca Perniola1
1CEA-Leti, France; 2STMicroelectronics, France

11:30 Characterization of Anomalous Random Telegraph Noise in Resistive Random Access Memory
Francesco Maria Puglisi, Luca Larcher, Andrea Padovani, Paolo Pavan
Università di Modena e Reggio Emilia, Italy

11:50 Improving the Resistive Switching Uniformity of Forming-Free TiO2-X Based Devices by Embedded Pt Nanocrystals
Panagiotis Bousoulas, Dionysis Sakellaropoulos, Jason Giannopoulos, Dimitris Tsoukalas
National Technical University of Athens, Greece
Thursday, September 17

Invited Session: Sensors and MEMS Applications

Session Code: C2L-G
Location: Villach
Time: 11:00 - 12:10
Chair(s): Christoph Kutter; Fraunhofer EMFT

10:50 Environmental Sensing in New Markets & Applications - Opportunities and Challenges for BME680 to Develop the Internet of Things
Thomas Block
Bosch Sensortec GmbH, Austria

11:10 Implications of Functional Safety on Future Sensor Concepts
Markus Foerste
Infineon Technologies AG, Austria

11:30 How Standardised MEMS Technology Platforms Can Enable Development and Manufacturing of Custom MEMS Products
Stephane Renard
Tronics Microsystems, Austria

11:50 Optical Sensors and Integration
Ingrid Jonak-Auer, Hubert Enichlmair, Gerhard Eimsteiner, Karl Rohracher, Martin Schrems
ams AG, Austria
Thursday, September 17

ESSDERC Plenary - T. Ernst

Session Code: C3L-D
Location: Klagenfurt
Time: 13:20 - 14:00
Chair(s): Tibor Grasser; Vienna University of Technology

13:20 High Performance NEMS Devices for Sensing Applications
Thomas Ernst, Sébastien Hentz, Julien Arcamone, Vincent Agache, Laurent Duraffourg, Issam Ouerghi, Willy Ludurczak, Carine Ladner, Eric Ollier, Philippe Andreucci, Eric Colinet, Pierre Puget

1APIX Analytics, France; 2CEA-Leti, France; 3CEA-Leti / Université Grenoble Alpes, France
Invited Session: Advanced Biomedical Devices

Session Code: C4L-C
Location: Klagenfurt
Time: 14:00 - 15:20
Chair(s): Roland Thewes; TU Berlin

14:00 New Frontiers in Digital Health: Remote Monitoring of Animal and Human Metabolism on Our Smartphones and Tablets
Sandro Carrara
École Polytechnique Fédérale de Lausanne, Switzerland

14:40 All-Digital Biomedical Imaging
Edoardo Charbon
Delft University of Technology, Netherlands
Thursday, September 17

Characterization of Advanced Devices

Session Code: C4L-E
Location: Linz
Time: 14:00 - 15:40
Chair(s): Gabriella Ghidini; STMicroelectronics
Sorin Cristoloveanu; Grenoble INP

14:00 Back-Gate Effects and Detailed Characterization of Junctionless Transistor
Mukta Singh Parihar3, Fan Yu Liu3, Carlos Navarro3, Sylvain Barraud1, Maryline Bawedin3, Irina Ionica3, Abhinav Kranti4, Sorin Cristoloveanu2
1CEA-Leti, France; 2Grenoble Polytechnic Institute / IMEP-LAH, France; 3IMEP-LAH, INP Grenoble, France; 4Indian Institute of Technology Indore, India

14:20 Low-Frequency Noise in Bare SOI Wafers: Experiments and Model
Luca Pirro2, Irina Ionica3, Sorin Cristoloveanu1, Gérard Ghibaudo2
1Grenoble Polytechnic Institute / IMEP-LAH, France; 2IMEP-LAH, France

14:40 Thin-Film SOI PIN-Diode Leakage Current Dependence on Back-Gate-Potential and HCI Traps
Andrei Schmidt, Stefan Dreiner, Holger Vogt, Uwe Paschen
Fraunhofer Institute for Microelectronic Circuits and Systems, IMS, Germany

15:00 H2 Annealing for Metallic Contaminant Reduction in BCD-SOI Process: Benefits and Drawbacks
Gabriella Ghidini, Daniele Merlini, Massimiliano Cannavo1, Maria Luisa Polignano, Isabella Mica, Amos Galbiati, Lucia Zullino, Riccardo Turconi, Salvatore Grasso, Maurizio Moroni, Davide Codegoni
STMicroelectronics, Italy

15:20 Contact Resistance Extraction Methods for CNTFETs
Anibal Pacheco-Sanchez2, Sven Mothes1, Martin Claus1, Michael Schröter2
1Technische Universität Dresden, Germany; 2Technische Universität Dresden, Germany
Advanced Numerical Modeling of Alternative Material Devices

Session Code: C4L-F
Location: Innsbruck
Time: 14:00 - 15:40
Chair(s): Denis Rideau; STMicroelectronics
Benjamin Iniguez; Universitat Rovira i Virgili, Spain

14:00 Analysis of InAs-Si Heterojunction Double-Gate Tunnel FETs with Vertical Tunneling Paths
Hamilton Carrillo-Nuñez, Mathieu Luisier, Andreas Schenk
ETH-Zürich, Switzerland

14:20 Improved Surface Roughness Modeling and Mobility Projections in Thin Film MOSFETs
Oves Badami, Enrico Caruso, Daniel Lizzit, David Esseni,
Pierpaolo Palestri, Luca Selmi
Università degli Studi di Udine, Italy

14:40 Predictive Physical Simulation of III/V Quantum-Well MISFETs for Logic Applications
Zlatan Stanojevic¹, Markus Karner¹, Martin Aichhorn³,
Ferdinand Mitterbauer¹, Volker Ewert², Christian Kernstock¹,
Hans Kosina³
¹Global TCAD Solutions GmbH, Austria; ²Materials Design, Inc., Germany; ³Technische Universität Wien, Austria

15:00 Strain Engineering of Single-Layer MoS2
Manouchehr Hosseini³, Mohammad Elahi³, Ebrahim Asl Soleimani²,
Mahdi Pourfath¹, David Esseni²
¹Technische Universität Wien, Austria; ²Università degli Studi di Udine, Italy; ³University of Tehran, Iran

15:20 Electric Performance of AlGaN/GaN Heterojunction Devices: a Full-Quantum Study
Luca Lucci¹, Jean-Charles Barbé¹, Marco Pala²
¹CEA-Leti, France; ²Université Grenoble Alpes, France
## Author Index

### A

<table>
<thead>
<tr>
<th>Name</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aghan, Vincent</td>
<td>101</td>
</tr>
<tr>
<td>Aguirre-Morales, Jorge Daniel</td>
<td>90</td>
</tr>
<tr>
<td>Aichhorn, Martin</td>
<td>104</td>
</tr>
<tr>
<td>Aihara, Takuma</td>
<td>84</td>
</tr>
<tr>
<td>Akinwande, Deji</td>
<td>90</td>
</tr>
<tr>
<td>Amat, Esteve</td>
<td>89</td>
</tr>
<tr>
<td>Ambacher, Oliver</td>
<td>81</td>
</tr>
<tr>
<td>Amoroso, Salvatore Maria</td>
<td>95, 97</td>
</tr>
<tr>
<td>Andreucci, Philippe</td>
<td>101</td>
</tr>
<tr>
<td>Arcamone, Julien</td>
<td>101</td>
</tr>
<tr>
<td>Asenov, Asen</td>
<td>95, 97</td>
</tr>
<tr>
<td>Asl Soleiman, Ebrahimi</td>
<td>104</td>
</tr>
<tr>
<td>Audoit, Guillaume</td>
<td>99</td>
</tr>
<tr>
<td>Aymerich, Xavier</td>
<td>95</td>
</tr>
<tr>
<td>Azzaz, Mourad</td>
<td>99</td>
</tr>
</tbody>
</table>

### B

<table>
<thead>
<tr>
<th>Name</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bablich, Andreas</td>
<td>90</td>
</tr>
<tr>
<td>Baccarani, Giorgio</td>
<td>87</td>
</tr>
<tr>
<td>Badami, Oves</td>
<td>104</td>
</tr>
<tr>
<td>Baek, Seung Beom</td>
<td>85</td>
</tr>
<tr>
<td>Bahat-Treidel, Eldad</td>
<td>81</td>
</tr>
<tr>
<td>Bain, James</td>
<td>84</td>
</tr>
<tr>
<td>Baltynov, Turar</td>
<td>86</td>
</tr>
<tr>
<td>Banerjee, Abhishek</td>
<td>81</td>
</tr>
<tr>
<td>Bansropun, Shailendra</td>
<td>88</td>
</tr>
<tr>
<td>Baravelli, Emanuele</td>
<td>87</td>
</tr>
<tr>
<td>Barbé, Jean-Charles</td>
<td>104</td>
</tr>
<tr>
<td>Barraud, Sylvain</td>
<td>94, 103</td>
</tr>
<tr>
<td>Barth, Edward</td>
<td>91</td>
</tr>
<tr>
<td>Bawedin, Maryline</td>
<td>103</td>
</tr>
<tr>
<td>Bazigos, Antonios</td>
<td>80</td>
</tr>
<tr>
<td>Bechen, Benjamin</td>
<td>93</td>
</tr>
<tr>
<td>Becherer, Markus</td>
<td>84</td>
</tr>
<tr>
<td>Beigne, Edith</td>
<td>89</td>
</tr>
<tr>
<td>Belete, Melkamu</td>
<td>94</td>
</tr>
<tr>
<td>Belmonte, Attilio</td>
<td>85</td>
</tr>
<tr>
<td>Benoist, Antoine</td>
<td>99</td>
</tr>
<tr>
<td>Bernasconi, Sophie</td>
<td>99</td>
</tr>
<tr>
<td>Bernstein, Gary</td>
<td>84</td>
</tr>
<tr>
<td>Berthou, Maxime</td>
<td>81</td>
</tr>
<tr>
<td>Bethge, Ole</td>
<td>81</td>
</tr>
<tr>
<td>Beyer, Volkhard</td>
<td>85</td>
</tr>
<tr>
<td>Billoint, Olivier</td>
<td>89</td>
</tr>
<tr>
<td>Biswas, Arnab</td>
<td>80</td>
</tr>
<tr>
<td>Blasco, Juli</td>
<td>80</td>
</tr>
<tr>
<td>Block, Thomas</td>
<td>100</td>
</tr>
<tr>
<td>Bodenstorfer, Ernst</td>
<td>93</td>
</tr>
</tbody>
</table>

### Boeuf, Frederic | 97 |
| Bösch, Wolfgang    | 93   |
| Boudre, Paul       | 96   |
| Bousoulas, Panagiotis | 99   |
| Breart de Boisanger, Michel | 88 |
| Breitkreutz-V. Gamm, Stephan | 84 |
| Brockherde, Werner  | 93   |
| Brodersen, Jörg     | 93   |
| Brunner, Frank      | 81   |
| Bury, Erik          | 95   |
| Buschbeck, Steffen  | 85   |

### C

<table>
<thead>
<tr>
<th>Name</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cagli, Carlo</td>
<td>99</td>
</tr>
<tr>
<td>Candelieri, Philippe</td>
<td>99</td>
</tr>
<tr>
<td>Cannavo’, Massimiliano</td>
<td>103</td>
</tr>
<tr>
<td>Capriotti, Mattia</td>
<td>81</td>
</tr>
<tr>
<td>Carrara, Sandro</td>
<td>102</td>
</tr>
<tr>
<td>Carrillo-Nuñez, Hamilto</td>
<td>104</td>
</tr>
<tr>
<td>Caruso, Enrico</td>
<td>104</td>
</tr>
<tr>
<td>Cassé, Mikaël</td>
<td>94</td>
</tr>
<tr>
<td>Catthoor, Francky</td>
<td>95</td>
</tr>
<tr>
<td>Caubet, Pierre</td>
<td>98</td>
</tr>
<tr>
<td>Chabane, Aziouz</td>
<td>88</td>
</tr>
<tr>
<td>Chae, Su Jin</td>
<td>85</td>
</tr>
<tr>
<td>Chalker, Paul</td>
<td>94</td>
</tr>
<tr>
<td>Charbon, Edoardo</td>
<td>102</td>
</tr>
<tr>
<td>Charpin, Christelle</td>
<td>99</td>
</tr>
<tr>
<td>Chen, An</td>
<td>85</td>
</tr>
<tr>
<td>Chen, Chao Yang</td>
<td>99</td>
</tr>
<tr>
<td>Cheng, Binjie</td>
<td>97</td>
</tr>
<tr>
<td>Chen, L</td>
<td>80</td>
</tr>
<tr>
<td>Cho, Moonju</td>
<td>95</td>
</tr>
<tr>
<td>Christmann, Jean-Frédéric</td>
<td>89</td>
</tr>
<tr>
<td>Claus, Martin</td>
<td>103</td>
</tr>
<tr>
<td>Clément, Nicolas</td>
<td>94</td>
</tr>
<tr>
<td>Codegoni, Davide</td>
<td>103</td>
</tr>
<tr>
<td>Colinet, Eric</td>
<td>101</td>
</tr>
<tr>
<td>Colombeau, Benjamin</td>
<td>94</td>
</tr>
<tr>
<td>Constant, Aurore</td>
<td>81</td>
</tr>
<tr>
<td>Coppens, P.</td>
<td>81</td>
</tr>
<tr>
<td>Couso, Carlos</td>
<td>95</td>
</tr>
<tr>
<td>Cristoloveanu, Sorin</td>
<td>86, 98, 103</td>
</tr>
<tr>
<td>Csaba, Gyorgy</td>
<td>84</td>
</tr>
</tbody>
</table>

### D

<table>
<thead>
<tr>
<th>Name</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dabertrand, Karen</td>
<td>98</td>
</tr>
<tr>
<td>Daves, Walter</td>
<td>81</td>
</tr>
<tr>
<td>Declercq, Frederick</td>
<td>81</td>
</tr>
</tbody>
</table>
Author Index

Degrave, Robin .................. 95, 99
De Micheli, Giovanni .......... 80
De Michielis, Luca .............. 80
Denorme, Stéphane ............. 99
Dentoni Litta, Eugenio ........ 94
De Schepper, Luc ............... 81
Deutschmann, Bernd .......... 86
De Vleeschouwer, Herbert .... 81
Dewolf, Tristan ................. 99
Dhanak, Vin ..................... 94
Dickmann, Jürgen ............... 79
Ding, Jie .......................... 97
Domengie, Florian .............. 98
Doris, Bruce B ................... 89
Dreiner, Stefan .................. 103
Duesberg, Georg ................. 92
Duraffourg, Laurent .......... 88, 101
Dutto, Christian ................. 86

G
Gaben, Loic .......................... 97
Gahoi, Amit ....................... 90
Gaillardon, Pierre-Emmanuel .... 80
Galiati, Amos ..................... 103
Gamiz, Francisco ............... 95
Ganguly, Swaroop .............. 94
Garin, Daniele .................. 99
Gatsbys, Riley .................... 92
Gergaud, Patrice ................ 88
Gerrr, Louis ...................... 95, 97
Ghibaudo, Gerard ............... 97, 98
Ghibaudo, Gérad ............... 103
Ghidini, Gabriella .............. 103
Giannopoulos, Jason .......... 99
Giebfried, Andrew ............. 84
Gnani, Elena ..................... 87
Gnudi, Antonio ................... 87
Godignon, Philippe ............. 81
Goes, Wolfgang ................ 95
Goiffon, Vincent ............... 88
Golanski, Dominique .......... 86
Gourlat, Guillaume ............. 88
Goux, Ludovic ................. 85, 99
Grassier, Tibor ................. 81, 90, 95
Grasso, Salvatore .............. 103
Greiner, Philipp ............... 86
Groesenenke, Guido .......... 95, 99
Groseringer, Jasmin .......... 93
Gross, Hannes ................. 93
Guedj, Cyril ...................... 99
Guerfi, Youssef ................. 94
Günther, Stefan ............... 85, 86
Guo, Jia .......................... 81

F
Fantini, Andrea .................. 85, 99
Faynot, Olivier .................. 94
Fenouillet-Beranger, Claire .... 99
Ferrari, Philippe ................. 98
Fian, Alexander ................. 96
Fleury, Clément ................. 81
Foerste, Markus ............... 100
Fonteneau, Pascal .............. 98
Fox, Alexander ................ 95
Franco, Jacopo ................. 95, 97
Fregonese, Sébastien .......... 90
Frégonèse, Sébastien .......... 90
Fukuda, Mitsuo .................. 84
Fukuhara, Masashi ............. 84

H
Hallam, Toby .................... 92
Hall, Steve ...................... 94
Hansryd, Jonas .................. 87
Han, Xiang-Lei ................. 94
Haond, Michel ................. 98
Happy, Henri .................... 90
Hentz, Sébastien ............... 88, 101
Heo, Chan ....................... 86
Hepp, David ..................... 94
Hiblot, Gaspard ................. 97
Hiit, Oliver ...................... 81
Hirano, Takuichi ............... 98
Hofbauer, Michael ............. 86

106  45th European Solid-State Device Research Conference • 2015
Hoffmann, Raik ................................ 85
Holweg, Gerald ................................ 86
Hook, Terence ................................ 89
Horiguchi, Naoto............................... 95, 97
Hosseini, Manouchehr......................... 104
Houssa, Michel................................ 85
Hubac, Stephane.............................. 91
Hussin, Razadi................................. 95, 97

I
Idrissi-El Oudhriri, Anouar ................. 88
Ikeda, Keiji .................................. 98
Illarionov, Yury ................................ 90
Inoue, Takeshi ................................ 98
Ionica, Irina.................................... 103
Irimia-Vladu, Mihai......................... 96
Ishii, Yuya ..................................... 84
Ishiyama, Takeshi.............................. 84

J
Jalaguier, Eric .................................. 99
Jauss, Simon ................................... 81
Jeannot, Simon ................................ 99
Jeon, Woochul .................................. 81
Jin, Jidong ...................................... 94
Joishi, Chandan................................. 94
Jonak-Auer, Ingrid............................. 100
Joseph, Vincent................................. 98
Jourdan, Guillaume......................... 88
Jo, Young-Woo ................................. 86
Jurczak, Malgorzata .......................... 85, 99

K
Kaczer, Ben.................................... 95, 97
Kaestner, Andre................................ 91
Kang, In Man ................................... 86
Karner, Esther ................................ 96
Karner, Markus................................. 104
Katariya, Satender ............................. 90
Kernstock, Christian......................... 104
Khanmohammadi, Abbas ..................... 86
Kim, Hyeong Soo.............................. 85
Kim, Hye-Young............................... 92
Kim, Jin Su .................................... 86
Kim, Joon-Seok................................. 90
Kim, Ryun-Hwi ................................. 86
Kimura, Yu ..................................... 84
Kollegger, Carolin......................... 86, 107
Kosina, Hans .................................. 104
Kothari, Shraddha ......................... 94, 95
Kraft, Jochen .................................. 91
Krant, Abhinav ................................ 103
Kukner, Halil .................................. 95

L
Ladner, Carine ................................. 88, 101
Lancaster, Suzanne ......................... 81
Laplanche, Yves ............................. 82
Larcher, Luca .................................. 99
Larrieu, Guilhem............................... 94
Le Baillif, Matthieu ......................... 88
Lee, Byoung Ki ............................... 85
Lee, Jong Chul ................................. 85
Lee, Jung-Hee ................................. 86
Lee, Min Yong ................................. 85
Lee, Young Ho ................................. 85
Lemme, Max .................................. 90, 94
Leroux, Charles............................... 98
Leteinturier, Patrick......................... 79
Li, Ning ......................................... 98
Linten, Dimitri ............................... 95
Litty, Antoine ................................. 86
Liu, Charlie .................................. 81
Liu, Fan Yu ................................. 103, 104
Li, Zilan ......................................... 81
Lizzit, Daniel .................................. 104
Lodha, Saurabh ............................... 94
Lucci, Luca................................. 104
Ludurczak, Willy ......................... 88, 101
Luisier, Mathieu......................... 104, 105
Lundstrom, Mark............................. 80
Lupina, Grzegorz ............................. 94

M
Magnan, Pierre............................... 88
Mai, Andreas .................................. 95
Maiti, T. K. .................................. 80
Maneux, Cristel............................... 90
Mano, Takehiro ......................... 84, 104
Marquez, Carlos .............................. 95
Martin-Martinez, Javier..................... 95
Martins, Paolo ............................... 88
Matsuzawa, Akira ......................... 98, 99
Mattausch, H. J................................ 80
Mayer, Konrad ................................ 93
McEvoy, Niall................................. 92
Merlin, Daniele......................... 103, 104
Author Index

Mica, Isabella .......................... 103
Mihai Ionescu, Adrian .................. 80
Mihaila, Andrei .......................... 81
Mikolajick, Thomas .................... 85
Millán, Jose .................................. 81
Miranda, Enrique ......................... 80
Mitrovic, Ivona .............................. 94
Mitterbauer, Ferdinand .................. 104
Miura-Mattausch, M ...................... 80
Miyamoto, H ............................... 80
Moens, Peter .................................. 81
Monfray, Stephane ....................... 82
Montserrat, Josep ......................... 81
Morche, Dominique ...................... 89
Moroni, Maurizio ........................... 103
Mothes, Sven ................................. 103
Muehlmann, Ulrich ....................... 93
Mukherjee, Chhandak ..................... 90

N
Nafria, Montserrat .......................... 95
Navarro, Carlos ............................ 103
Nejad, Hasan ............................... 94
Niquet, Yann-Michel ...................... 94
Nitta, Christian .............................. 93
Noll, Stefan .................................. 81

O
O’Brien, Maria .............................. 92
Ocker, Johannes ......................... 85
Okada, Kenichi .............................. 98
Ollier, Eric .................................. 101
Orlov, Alexei .................................. 84
Ortolland, Sylvie ............................. 86
Ostermaier, Clemens ...................... 81
Östling, Mikael .............................. 90, 94
Ota, Masashi .................................. 84
Ouerghi, Issam ............................... 88, 101

P
Pacheco-Sanchez, Anibal .................. 103
Padmanabhan, Balaji ...................... 81
Padovani, Andrea ........................... 99
Pala, Marco .................................. 104
Palestri, Pierpaolo ......................... 104
Pang, Jian .................................. 98
Papp, Adam .................................. 84
Parihar, Mukta Singh ...................... 103
Park, Hae Chan .............................. 85
Paschen, Uwe ............................... 103
Passi, Vikram ............................... 90
Pavan, Paolo ................................. 99
Pelamatti, Alice ............................. 88
Pelloux-Prayer, Johan .................. 94
Perniola, Luca ............................... 99
Petritz, Andreas ............................. 96
Pirro, Luca .................................. 103
Pobegen, Gregor ........................... 81
Pogány, Dionyz ............................. 81
Polignano, Maria Luisa .................. 103
Porod, Wolfgang ......................... 84
Porti, Marc ................................. 95
Pourfath, Mahdi ............................. 104
Puget, Pierre ................................. 101

R
Rafhay, Quentin ............................ 97
Raghavan, Praveen ....................... 95
Raskin, Jean-Pierre ....................... 82
Rebollo, Jose ................................. 81
Redolfi, Augusto ............................ 85, 99
Reggiani, Susanna ....................... 87
Reid, Dave .................................. 97
Reimbild, Gilles ............................. 94, 98
Renard, Stephane ......................... 100
Rigato, Matteo .............................. 81
Rodriguez, Rosana ....................... 95
Rohracher, Karl ............................. 100
Romano, Giovanni ....................... 98
Roussel, Philippe ........................... 95
Rouvière, Jean-Luc ...................... 94
Rzepe, Gerhard ............................. 95

S
Saint-Pé, Olivier ........................... 88
Saitoh, Masumi .............................. 98
Sakai, Hiroki ................................. 84
Sakane, Hitoshi ............................. 98
Sakellaropoulos, Dionysios .............. 99
Salih, A ...................................... 81
Sansa, Marc ................................. 88
Sansen, Willy ................................. 79
Schenk, Andreas ......................... 104
Schmidt, Andrei ............................ 103
Schmitt-Landsiedel, Doris .............. 84
Schrank, Franz .............................. 91
Schremes, Martin ......................... 91, 100
<table>
<thead>
<tr>
<th>Author</th>
<th>Year</th>
</tr>
</thead>
<tbody>
<tr>
<td>Schrey, Olaf</td>
<td>93</td>
</tr>
<tr>
<td>Schröter, Michael</td>
<td>103</td>
</tr>
<tr>
<td>Schwaiger, Stephan</td>
<td>81</td>
</tr>
<tr>
<td>Selmi, Luca</td>
<td>104</td>
</tr>
<tr>
<td>Seo, Jae Hwa</td>
<td>86</td>
</tr>
<tr>
<td>Sharma, Abhishek</td>
<td>84</td>
</tr>
<tr>
<td>Shaw, Andrew</td>
<td>94</td>
</tr>
<tr>
<td>Sicard, Gilles</td>
<td>88</td>
</tr>
<tr>
<td>Simicic, Marco</td>
<td>95, 97</td>
</tr>
<tr>
<td>Skotnicki, Thomas</td>
<td>82</td>
</tr>
<tr>
<td>Skowronski, Marek</td>
<td>84</td>
</tr>
<tr>
<td>Slesazeck, Stefan</td>
<td>85</td>
</tr>
<tr>
<td>Smith, Anderson</td>
<td>90, 94</td>
</tr>
<tr>
<td>Solano, Yohann</td>
<td>98</td>
</tr>
<tr>
<td>Soler, Victor</td>
<td>81</td>
</tr>
<tr>
<td>Son, Dong-Hyeok</td>
<td>86</td>
</tr>
<tr>
<td>Spreitzer, Raphael</td>
<td>93</td>
</tr>
<tr>
<td>Stadlober, Barbara</td>
<td>96</td>
</tr>
<tr>
<td>Stanojevic, Zlatan</td>
<td>104</td>
</tr>
<tr>
<td>Steffan, Christoph</td>
<td>86</td>
</tr>
<tr>
<td>Stradiotto, Roberta</td>
<td>81</td>
</tr>
<tr>
<td>Strasser, Gottfried</td>
<td>81</td>
</tr>
<tr>
<td>Streiff, Matthias</td>
<td>93</td>
</tr>
<tr>
<td>Strle, Drago</td>
<td>93</td>
</tr>
<tr>
<td>Suarez-Segovia, Carlos</td>
<td>98</td>
</tr>
<tr>
<td>Suñé, Jordi</td>
<td>80</td>
</tr>
<tr>
<td>Szakmany, Gergo</td>
<td>84</td>
</tr>
<tr>
<td>Tack, M.</td>
<td>81</td>
</tr>
<tr>
<td>Takagi, Shinichi</td>
<td>83</td>
</tr>
<tr>
<td>Takenaka, Mitsuru</td>
<td>83</td>
</tr>
<tr>
<td>Tanaka, Chika</td>
<td>98</td>
</tr>
<tr>
<td>Tao, Li</td>
<td>90</td>
</tr>
<tr>
<td>Triozon, François</td>
<td>94</td>
</tr>
<tr>
<td>Trontelj, Janez</td>
<td>93</td>
</tr>
<tr>
<td>Tsoukalas, Dimitris</td>
<td>99</td>
</tr>
<tr>
<td>Turconi, Riccardo</td>
<td>103</td>
</tr>
<tr>
<td>Vaziri, Sam</td>
<td>90, 94</td>
</tr>
<tr>
<td>Velayudhan, Vikas</td>
<td>95</td>
</tr>
<tr>
<td>Vianello, Elisa</td>
<td>99</td>
</tr>
<tr>
<td>Villard, Patrick</td>
<td>88</td>
</tr>
<tr>
<td>Vinet, Maud</td>
<td>88</td>
</tr>
<tr>
<td>Virmontois, Cédric</td>
<td>88</td>
</tr>
<tr>
<td>Vogt, Holger</td>
<td>103</td>
</tr>
<tr>
<td>Wagner, Stefan</td>
<td>90</td>
</tr>
<tr>
<td>Waltl, Michael</td>
<td>90</td>
</tr>
<tr>
<td>Wang, Liping</td>
<td>97</td>
</tr>
<tr>
<td>Weber, Olivier</td>
<td>98</td>
</tr>
<tr>
<td>Weckx, Pieter</td>
<td>95, 97</td>
</tr>
<tr>
<td>Wei, Wei</td>
<td>90</td>
</tr>
<tr>
<td>Weldon, Jeffrey</td>
<td>84</td>
</tr>
<tr>
<td>Whittles, Thomas</td>
<td>94</td>
</tr>
<tr>
<td>Wrench, Jacqueline</td>
<td>89</td>
</tr>
<tr>
<td>Würfl, Joachim</td>
<td>81</td>
</tr>
<tr>
<td>Wu, Rui</td>
<td>98</td>
</tr>
<tr>
<td>Yeniceri, Ramazan</td>
<td>84</td>
</tr>
<tr>
<td>Yurchuk, Ekatarina</td>
<td>85</td>
</tr>
<tr>
<td>Zhang, Jian</td>
<td>80</td>
</tr>
<tr>
<td>Zhu, Weinan</td>
<td>90</td>
</tr>
<tr>
<td>Ziaei, Afshin</td>
<td>88</td>
</tr>
<tr>
<td>Žiemys, Gražvydas</td>
<td>84</td>
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